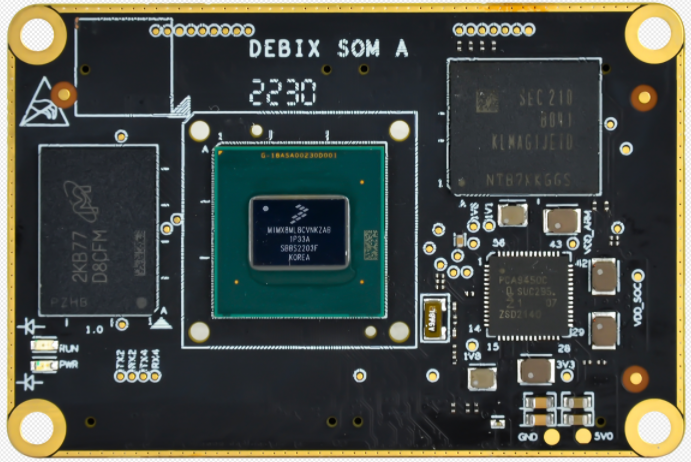
**DEBIX SOM A Datasheet**

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**Chapter 1 DEBIX SOM A introduction**

DEBIX SOM A is an embedded SOM(System on Module) board based on NXP i.MX 8M Plus. It can choose to use the commercial grade CPU or the industrial grade CPU, which focuses on machine learning and vision, advanced multimedia, and industrial automation with high reliability.

Main features:

* Have powerful quad-core Arm® Cortex®-A53 CPU, have the NPU which operates at up to 2.3TOPS
* Dual image signal processors(ISP) and two camera inputs for an effective Vision System
* The multimedia capabilities include video encode(including H.265, H.264) and video decode(including H.265, H.264),3D/2D graphic acceleration, and multiple audio and voice functionalities.
* Real-time control with Cortex-M7. Robust control networks supported by dual CAN FD(IT version) and dual Gigabit Ethernet, one of which support Time Sensitive Networking(TSN).
* High industrial reliability with DRAM inline ECC
* Designed for critical environment condition and temperature change, the wide CPU temperature range -40℃ ~105℃ make it can be used in critical industrial environment, transportation and industry control etc.
* Support Ubuntu, Android, Yocto

Feature summary:

* System
* CPU: NXP i.MX 8M Plus(default), 4 x Cortex-A53, with NPU operating at 2.3TOPS, Industrial grade CPU runs at 1.6GHz, Commercial grade CPU runs at 1.8GHz(i.MX 8M Plus whole series CPU optional)
* RAM: 2GB LPDDR4(1GB/4GB/6GB/8GB optional)
* Flash: on-board 16GB eMMC(8GB/32GB/64GB/128GB/256GB optional)
* Operating System: Ubuntu20.04, Android11, Yocto-L5.10.72\_2.2.0
* I/O interface:
* Ethernet: 2 x Gigabyte Ethernet controller, one of which support Time sensitive Network(TSN)
* Display: 1 x HDMI2.0a, support 1920x1080p60, 1920x1080p120, 3840x2160p30 etc.

1 x LVDS, support 4-lane and 8-lane

1 x MIPI DSI, support 2560 x 1080 60Hz

* Camera: 2 x MIPI CSI
* Audio: Up to 6 x SAI(synchronous audio interface), HiFi4 DSP, 1x SPDIF IN, 1xSPDIF OUT(Note: 1 x SAI with 8 TX and 8 RX lanes, 1 x SAI with 4 TX and 4 RX lanes, 2 x SAI with 2 TX and 2 RX lanes, 2 x SAI with 1 TX and 1 RX lane, all SAIs support I2S and AC97)
* USB: 2 x USB3.0, can be configured as device and host
* UART: up to 4 x UART
* I2C: up to 6 x I2C, I2C2~I2C6 are exposed to the connectors(2 of the five I2Cs are multiplexed as SD1), I2C1 is not allowed to be configured.
* SDIO: 2xSDIO
* SPI: up to 3 x ECSPI
* PCIe: 1 x PCIe Gen3
* CAN: 2 x CAN
* GPIO: 13 x GPIO by default, other functional pins can be configured as GPIO through software
* Power :
* Input voltage: 3.5V~5V
* CPU working temperature:
* Consumer grade: 0℃~95℃
* Industrial grade:-40℃~105℃
* Mechanical:
* Connector: 4 double-sided board-to-board plug connector, the model of which is BB51024A-R80-10-32, 2 x 40pin/0.5mm pitch
* Dimension: 60mm(length) x 40mm(width) x 5.6mm(height)

**Chapter 2 Main hardware Construction**

The main components of DEBIX SOM A are introduced in this chapter.

**2.1 CPU (NXP i.MX 8MP Plus)**

NXP i.MX 8M Plus meets the needs of smart family, smart city and industrial 4.0 application.

**2.2 Storage**

* RAM: 2GB LPDDR4(1GB/4GB/6GB/8GB optional)
* Flash: on-board 16GB eMMC by default(8GB/32GB/64GB/128GB/256GB optional)

**2.3 PMIC**

The Power Management IC(PMIC) that DEBIX SOM A used is PCA9450C.

**Chapter 3 External Connectors**

**3.1 board-to-board connector**

DEBIX SOM A exposes 4 board-to-bard plug connectors, the model of which is BB51024A-R80-10-32, 2 x 40pin/0.5mm pitch, matching 4 Socket connectors with different heights, the models are BB51024W-R80-30-32, BB15024W-R80-35-32, BB15024W-R80-40-32, BB15024W-R80-45-32.

**3.2 Connector Pinout**

The following tables list the pinout of the four connectors, the corresponding CPU pin name are also given.

The table header instructions are described as below:

* Default: Functional definition we used(Defined in schematics)
* BALL\_NAME: CPU pin name of the corresponding pin
* BALL: CPU pin serial number

**3.2.1 DEBIX SOM A J3 Pinout**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Location** | **PIN** | **Default** | **BALL\_NAME** | **BALL** | **NOTES** |
| J3 | Pin1 | GND |  |  |  |
| J3 | Pin2 | GND |  |  |  |
| J3 | Pin3 | GPIO1\_IO06 | GPIO1\_IO06 | A3 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin4 | GPIO1\_IO15 | GPIO1\_IO15 | B5 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin5 | GPIO1\_IO05 | GPIO1\_IO05 | B4 | NVCC\_GPIO, 1V8, Output high during reset, input with PU after reset |
| J3 | Pin6 | GPIO1\_IO14 | GPIO1\_IO14 | A4 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin7 | GPIO1\_IO01 | GPIO1\_IO01 | E8 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset |
| J3 | Pin8 | GPIO1\_IO13 | GPIO1\_IO13 | A6 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin9 | GPIO1\_IO00 | GPIO1\_IO00 | A7 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin10 | GPIO1\_IO12 | GPIO1\_IO12 | A5 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin11 | GND |  |  |  |
| J3 | Pin12 | GPIO1\_IO11 | GPIO1\_IO11 | D8 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin13 | USB1\_RXN | USB1\_RX\_N | B9 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin14 | GPIO1\_IO10 | GPIO1\_IO10 | B7 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin15 | USB1\_RXP | USB1\_RX\_P | A9 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin16 | GPIO1\_IO09 | GPIO1\_IO09 | B8 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin17 | GND |  |  |  |
| J3 | Pin18 | GPIO1\_IO08 | GPIO1\_IO08 | A8 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin19 | USB1\_TXN | USB1\_TX\_N | B10 | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin20 | GPIO1\_IO07 | GPIO1\_IO07 | F6 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin21 | USB1\_TXP | USB1\_TX\_P | A10 | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin22 | GND |  |  |  |
| J3 | Pin23 | GND |  |  |  |
| J3 | Pin24 | USB1\_DN | USB1\_D\_N | E10 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin25 | USB2\_RXN | USB2\_RX\_N | B12 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin26 | USB1\_DP | USB1\_D\_P | D10 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin27 | USB2\_RXP | USB2\_RX\_P | A12 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin28 | GND |  |  |  |
| J3 | Pin29 | GND |  |  |  |
| J3 | Pin30 | USB2\_DN | USB2\_D\_N | E14 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin31 | USB2\_TXN | USB2\_TX\_N | B13 | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin32 | USB2\_DP | USB2\_D\_P | D14 | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin33 | USB2\_TXP | USB2\_TX\_P | A13 | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin34 | GND |  |  |  |
| J3 | Pin35 | GND |  |  |  |
| J3 | Pin36 | USB1\_VBUS\_3V3 | USB1\_VBUS | A11 | VDD\_USB\_3P3, 3.3V, Input |
| J3 | Pin37 | PCIE\_CLKN | PCIE\_REF\_PAD\_CLK\_N | E16 | VDD\_PCI\_1P8, 1V8, High-Z |
| J3 | Pin38 | USB2\_VBUS\_3V3 | USB2\_VBUS | D12 | VDD\_USB\_3P3, 3.3V, Input |
| J3 | Pin39 | PCIE\_CLKP | PCIE\_REF\_PAD\_CLK\_P | D16 | VDD\_PCI\_1P8, 1V8, High-Z |
| J3 | Pin40 | JTAG\_TMS | JTAG\_TMS | G14 | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin41 | GND |  |  |  |
| J3 | Pin42 | JTAG\_TDO | JTAG\_TDO | F14 | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin43 | PCIE\_RXN | PCIE\_RXN\_N | B14 | VDD\_PCI\_1P8, 1V8, Input, High-Z |
| J3 | Pin44 | JTAG\_TDI | JTAG\_TDI | G16 | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin45 | PCIE\_RXP | PCIE\_RXN\_P | A14 | VDD\_PCI\_1P8, 1V8, Input, High-Z |
| J3 | Pin46 | JTAG\_MOD | JTAG\_MOD | G20 | NVCC\_JTAG, 1V8, Input with PD |
| J3 | Pin47 | GND |  |  |  |
| J3 | Pin48 | JTAG\_TCK | JTAG\_TCK | G18 | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin49 | PCIE\_TXN | PCIE\_TXN\_N | B15 | VDD\_PCI\_1P8, 1V8, Output, High-Z |
| J3 | Pin50 | GND |  |  |  |
| J3 | Pin51 | PCIE\_TXP | PCIE\_TXN\_P | A15 | VDD\_PCI\_1P8, 1V8, Output, High-Z |
| J3 | Pin52 | CSI1\_DN0 | MIPI\_CSI1\_D0\_N | E18 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin53 | GND |  |  |  |
| J3 | Pin54 | CSI1\_DP0 | MIPI\_CSI1\_D0\_P | D18 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin55 | DSI\_DN0 | MIPI\_DSI1\_D0\_N | B16 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin56 | GND |  |  |  |
| J3 | Pin57 | DSI\_DP0 | MIPI\_DSI1\_D0\_P | A16 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin58 | CSI1\_DN1 | MIPI\_CSI1\_D1\_N | E20 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin59 | DSI\_DN1 | MIPI\_DSI1\_D1\_N | B17 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin60 | CSI1\_DP1 | MIPI\_CSI1\_D1\_P | D20 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin61 | DSI\_DP1 | MIPI\_DSI1\_D1\_P | A17 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin62 | GND |  |  |  |
| J3 | Pin63 | GND |  |  |  |
| J3 | Pin64 | CSI1\_CKN | MIPI\_CSI1\_CLK\_N | E22 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin65 | DSI\_CKN | MIPI\_DSI1\_CLK\_N | B18 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin66 | CSI1\_CKP | MIPI\_CSI1\_CLK\_P | D22 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin67 | DSI\_CKP | MIPI\_DSI1\_CLK\_P | A18 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin68 | GND |  |  |  |
| J3 | Pin69 | GND |  |  |  |
| J3 | Pin70 | CSI1\_DN2 | MIPI\_CSI1\_D2\_N | E24 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin71 | DSI\_DN2 | MIPI\_DSI1\_D2\_N | B19 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin72 | CSI1\_DP2 | MIPI\_CSI1\_D2\_P | D24 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin73 | DSI\_DP2 | MIPI\_DSI1\_D2\_P | A19 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin74 | GND |  |  |  |
| J3 | Pin75 | DSI\_DN3 | MIPI\_DSI1\_D3\_N | B20 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin76 | CSI1\_DN3 | MIPI\_CSI1\_D3\_N | E26 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin77 | DSI\_DP3 | MIPI\_DSI1\_D3\_P | A20 | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin78 | CSI1\_DP3 | MIPI\_CSI1\_D3\_P | D26 | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin79 | GND |  |  |  |
| J3 | Pin80 | GND |  |  |  |

**3.2.2 DEBIX SOM A J4 pinout**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Location** | **PIN** | **Default** | **BALL\_NAME** | **BALL** | **NOTES** |
| J4 | Pin1 | GND |  |  |  |
| J4 | Pin2 | GND |  |  |  |
| J4 | Pin3 | LVDS1\_TX0\_P | LVDS1\_D0\_P | A26 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin4 | CSI2\_DN3 | MIPI\_CSI2\_D3\_N | B21 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin5 | LVDS1\_TX0\_N | LVDS1\_D0\_N | B26 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin6 | CSI2\_DP3 | MIPI\_CSI2\_D3\_P | A21 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin7 | GND |  |  |  |
| J4 | Pin8 | GND |  |  |  |
| J4 | Pin9 | LVDS1\_TX1\_P | LVDS1\_D1\_P | A27 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin10 | CSI2\_DN2 | MIPI\_DSI2\_D2\_N | B22 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin11 | LVDS1\_TX1\_N | LVDS1\_D1\_N | B27 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin12 | CSI2\_DP2 | MIPI\_DSI2\_D2\_P | A22 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin13 | GND |  |  |  |
| J4 | Pin14 | GND |  |  |  |
| J4 | Pin15 | LVDS1\_CLK\_P | LVDS1\_CLK\_P | A28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin16 | CSI2\_CKN | MIPI\_CSI2\_CLK\_N | B23 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin17 | LVDS1\_CLK\_N | LVDS1\_CLK\_N | B28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin18 | CSI2\_CKP | MIPI\_CSI2\_CLK\_P | A23 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin19 | GND |  |  |  |
| J4 | Pin20 | GND |  |  |  |
| J4 | Pin21 | LVDS1\_TX2\_P | LVDS1\_D2\_P | B29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin22 | CSI2\_DN1 | MIPI\_CSI2\_D1\_N | B24 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin23 | LVDS1\_TX2\_N | LVDS1\_D2\_N | C28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin24 | CSI2\_DP1 | MIPI\_CSI2\_D1\_P | A24 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin25 | GND |  |  |  |
| J4 | Pin26 | GND |  |  |  |
| J4 | Pin27 | LVDS1\_TX3\_P | LVDS1\_D3\_P | C29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin28 | CSI2\_DN0 | MIPI\_CSI2\_D0\_N | B25 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin29 | LVDS1\_TX3\_N | LVDS1\_D3\_N | D28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin30 | CSI2\_DP0 | MIPI\_CSI2\_D0\_P | A25 | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin31 | GND |  |  |  |
| J4 | Pin32 | GND |  |  |  |
| J4 | Pin33 | LVDS0\_TX0\_P | LVDS0\_D0\_P | D29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin34 | NAND\_DQS | NAND\_DQS | R26 | NVCC\_NAND, 1V8, Input with PD |
| J4 | Pin35 | LVDS0\_TX0\_N | LVDS0\_D0\_N | E28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin36 | ONOFF | ONOFF | G22 | NVCC\_SNVS, 1V8, Input with PU |
| J4 | Pin37 | GND |  |  |  |
| J4 | Pin38 | POR\_B | POR\_B | J29 | NVCC\_SNVS, 1V8, Input with PU |
| J4 | Pin39 | LVDS0\_TX1\_P | LVDS0\_D1\_P | E29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin40 | PMIC\_ON\_REQ | LVDS0\_D1\_P | F22 | NVCC\_SNVS, 1V8, Output high with PU |
| J4 | Pin41 | LVDS0\_TX1\_N | LVDS0\_D1\_N | F28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin42 | GND |  |  |  |
| J4 | Pin43 | GND |  |  |  |
| J4 | Pin44 | BOOT\_MODE0 | BOOT\_MODE0 | G10 | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin45 | LVDS0\_CLK\_P | LVDS0\_CLK\_P | F29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin46 | BOOT\_MODE1 | BOOT\_MODE1 | F8 | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin47 | LVDS0\_CLK\_N | LVDS0\_CLK\_N | G28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin48 | BOOT\_MODE2 | BOOT\_MODE2 | G8 | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin49 | GND |  |  |  |
| J4 | Pin50 | BOOT\_MODE3 | BOOT\_MODE3 | G12 | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin51 | LVDS0\_TX2\_P | LVDS0\_D2\_P | G29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin52 | WDOG\_B | GPIO1\_IO02 | B6 | NVCC\_GPIO, 1V8, Input with PU |
| J4 | Pin53 | LVDS0\_TX2\_N | LVDS0\_D2\_N | H28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin54 | GND |  |  |  |
| J4 | Pin55 | GND |  |  |  |
| J4 | Pin56 | CLKIN1 | CLKIN1 | K28 | NVCC\_CLK, 1V8, Input with PD |
| J4 | Pin57 | LVDS0\_TX3\_P | LVDS0\_D3\_P | H29 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin58 | GND |  |  |  |
| J4 | Pin59 | LVDS0\_TX3\_N | LVDS0\_D3\_N | J28 | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin60 | CLKOUT1 | CLKOUT1 | K29 | NVCC\_CLK, 1V8, Output low |
| J4 | Pin61 | GND |  |  |  |
| J4 | Pin62 | GND |  |  |  |
| J4 | Pin63 | SD1\_STROBE | SD1\_STROBE | W26 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin64 | CLKIN2 | CLKIN2 | L28 | NVCC\_CLK, 1V8, Input with PD |
| J4 | Pin65 | SD1\_RESET\_B | SD1\_RESET\_B | W25 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin66 | GND |  |  |  |
| J4 | Pin67 | SD1\_CLK | SD1\_CLK | W28 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin68 | CLKOUT2 | CLKOUT2 | L29 | NVCC\_CLK, 1V8, Output low |
| J4 | Pin69 | SD1\_CMD | SD1\_CMD | W29 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin70 | GND |  |  |  |
| J4 | Pin71 | SD1\_DATA0 | SD1\_DATA0 | Y29 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin72 | SD1\_DATA4 | SD1\_DATA4 | U26 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin73 | SD1\_DATA1 | SD1\_DATA1 | Y28 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin74 | SD1\_DATA5 | SD1\_DATA5 | AA29 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin75 | SD1\_DATA2 | SD1\_DATA2 | V29 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin76 | SD1\_DATA6 | SD1\_DATA6 | AA28 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin77 | SD1\_DATA3 | SD1\_DATA3 | V28 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin78 | SD1\_DATA7 | SD1\_DATA7 | U25 | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin79 | GND |  |  |  |
| J4 | Pin80 | GND |  |  |  |

**3.2.3 DEBIX SOM A J5 Pinout**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Location** | **PIN** | **Default** | **BALL\_NAME** | **BALL** | **NOTES** |
| J5 | Pin1 | GND |  |  |  |
| J5 | Pin2 | GND |  |  |  |
| J5 | Pin3 | I2C2\_SCL | I2C2\_SCL | AH6 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin4 | UART1\_TXD | UART1\_TXD | AJ3 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin5 | I2C2\_SDA | I2C2\_SDA | AE8 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin6 | UART1\_RXD | UART1\_RXD | AD6 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin7 | I2C3\_SCL | I2C3\_SCL | AJ7 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin8 | UART1\_CTS | UART3\_RXD | AE6 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin9 | I2C3\_SDA | I2C3\_SDA | AJ6 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin10 | UART1\_RTS | UART3\_TXD | AJ4 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin11 | I2C4\_SCL | I2C4\_SCL | AF8 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin12 | UART2\_TXD | UART2\_TXD | AH4 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin13 | I2C4\_SDA | I2C4\_SDA | AD8 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin14 | UART2\_RXD | UART2\_RXD | AF6 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin15 | GND |  |  |  |
| J5 | Pin16 | UART4\_TXD | UART4\_TXD | AH5 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin17 | SAI1\_TXC | SAI1\_TXC | AJ12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin18 | UART4\_RXD | UART4\_RXD | AJ5 | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin19 | SAI1\_TXD0 | SAI1\_TXD0 | AJ11 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin20 | GND |  |  |  |
| J5 | Pin21 | SAI1\_TXD1 | SAI1\_TXD1 | AJ10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin22 | SAI1\_RXFS | SAI1\_RXFS | AJ9 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin23 | SAI1\_TXD2 | SAI1\_TXD2 | AH11 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin24 | SAI1\_RXC | SAI1\_RXC | AH8 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin25 | SAI1\_TXD3 | SAI1\_TXD3 | AD12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin26 | SAI1\_RXD0 | SAI1\_RXD0 | AC10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin27 | SAI1\_TXD4 | SAI1\_TXD4 | AH13 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin28 | SAI1\_RXD1 | SAI1\_RXD1 | AF10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin29 | SAI1\_TXD5 | SAI1\_TXD5 | AH14 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin30 | SAI1\_RXD2 | SAI1\_RXD2 | AH9 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin31 | SAI1\_TXD6 | SAI1\_TXD6 | AC12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin32 | SAI1\_RXD3 | SAI1\_RXD3 | AJ8 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin33 | SAI1\_TXD7 | SAI1\_TXD7 | AJ13 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin34 | SAI1\_RXD4 | SAI1\_RXD4 | AD10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin35 | SAI1\_TXFS | SAI1\_TXFS | AF12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin36 | SAI1\_RXD5 | SAI1\_RXD5 | AE10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin37 | GND |  |  |  |
| J5 | Pin38 | SAI1\_RXD6 | SAI1\_RXD6 | AH10 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin39 | SAI5\_RXD0 | SAI5\_RXD0 | AE16 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin40 | SAI1\_RXD7 | SAI1\_RXD7 | AH12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin41 | SAI5\_RXD1 | SAI5\_RXD1 | AD16 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin42 | SAI1\_MCLK | SAI1\_MCLK | AE12 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin43 | SAI5\_RXD2 | SAI5\_RXD2 | AF16 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin44 | GND |  |  |  |
| J5 | Pin45 | SAI5\_RXD3 | SAI5\_RXD3 | AE14 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin46 | SAI5\_RXFS | SAI5\_RXFS | AC14 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin47 | SAI2\_TXC | SAI2\_TXC | AH15 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin48 | SAI5\_RXC | SAI5\_RXC | AD14 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin49 | SAI2\_TXFS | SAI2\_TXFS | AJ17 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin50 | SAI5\_MCLK | SAI5\_MCLK | AF14 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin51 | SAI2\_TXD | SAI2\_TXD0 | AH16 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin52 | SAI2\_RXFS | SAI2\_RXFS | AH17 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin53 | SAI2\_RXD | SAI2\_RXD0 | AJ14 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin54 | SAI2\_RXC | SAI2\_RXC | AJ16 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin55 | SAI3\_TXC | SAI3\_TXC | AH19 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin56 | SAI2\_MCLK | SAI2\_MCLK | AJ15 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin57 | SAI3\_TXFS | SAI3\_TXFS | AC16 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin58 | SAI3\_MCLK | SAI3\_MCLK | AJ20 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin59 | SAI3\_TXD | SAI3\_TXD | AH18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin60 | SAI3\_RXC | SAI3\_RXC | AJ18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin61 | GND |  |  |  |
| J5 | Pin62 | SAI3\_RXFS | SAI3\_RXFS | AJ19 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin63 | ECSPI2\_SCLK | ECSPI2\_SCLK | AH21 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin64 | SAI3\_RXD | SAI3\_RXD | AF18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin65 | ECSPI2\_SS0 | ECSPI2\_SS0 | AJ22 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin66 | SPDIF\_TX | SPDIF\_TX | AE18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin67 | ECSPI2\_MOSI | ECSPI2\_MOSI | AJ21 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin68 | SPDIF\_RX | SPDIF\_RX | AD18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin69 | ECSPI2\_MISO | ECSPI2\_MISO | AH20 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin70 | SPDIF\_EXT\_CLK | SPDIF\_EXT\_CLK | AC18 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin71 | HDMI\_DDC\_SCL | HDMI\_DDC\_SCL | AC22 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin72 | UART3\_CTS | ECSPI1\_MISO | AD20 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin73 | HDMI\_DDC\_SDA | HDMI\_DDC\_SDA | AF22 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin74 | UART3\_RTS | ECSPI1\_SS0 | AE20 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin75 | HDMI\_HPD | HDMI\_HPD | AE22 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin76 | UART3\_TXD | ECSPI1\_MOSI | AC20 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin77 | HDMI\_CEC | HDMI\_CEC | AD22 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin78 | UART3\_RXD | ECSPI1\_SCLK | AF20 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin79 | GND |  |  |  |
| J5 | Pin80 | GND |  |  |  |

**3.2.4 DEBIX SOM A J6 Pinout**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Location** | **PIN** | **Default** | **BALL\_NAME** | **BALL** | **NOTES** |
| J6 | Pin1 | GND |  |  |  |
| J6 | Pin2 | GND |  |  |  |
| J6 | Pin3 | EARC\_N\_HPD | EARC\_N\_HPD | AH22 | VDD\_EARC\_1P8, 1V8, Output |
| J6 | Pin4 | ENET\_MDC | ENET\_MDC | AH28 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin5 | EARC\_P\_UTIL | EARC\_P\_UTIL | AJ23 | VDD\_EARC\_1P8, 1V8, Output |
| J6 | Pin6 | ENET\_MDIO | ENET\_MDIO | AH29 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin7 | GND |  |  |  |
| J6 | Pin8 | ENET\_TX\_CTL | ENET\_TX\_CTL | AF24 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin9 | HDMI\_TXCN | HDMI\_TXC\_N | AJ24 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin10 | ENET\_TXC | ENET\_TXC | AE24 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin11 | HDMI\_TXCP | HDMI\_TXC\_P | AH24 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin12 | ENET\_TD0 | ENET\_TD0 | AC25 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin13 | GND |  |  |  |
| J6 | Pin14 | ENET\_TD1 | ENET\_TD1 | AE26 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin15 | HDMI\_TXN0 | HDMI\_TX0\_N | AJ25 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin16 | ENET\_TD2 | ENET\_TD2 | AF26 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin17 | HDMI\_TXP0 | HDMI\_TX0\_P | AH25 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin18 | ENET\_TD3 | ENET\_TD3 | AD24 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin19 | GND |  |  |  |
| J6 | Pin20 | ENET\_RX\_CTL | ENET\_RX\_CTL | AE28 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin21 | HDMI\_TXN1 | HDMI\_TX1\_N | AJ26 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin22 | ENET\_RXC | ENET\_RXC | AE29 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin23 | HDMI\_TXP1 | HDMI\_TX1\_P | AH26 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin24 | ENET\_RD0 | ENET\_RD0 | AG29 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin25 | GND |  |  |  |
| J6 | Pin26 | ENET\_RD1 | ENET\_RD1 | AG28 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin27 | HDMI\_TXN2 | HDMI\_TX2\_N | AJ27 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin28 | ENET\_RD2 | ENET\_RD2 | AF29 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin29 | HDMI\_TXP2 | HDMI\_TX2\_P | AH27 | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin30 | ENET\_RD3 | ENET\_RD3 | AF28 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin31 | GND |  |  |  |
| J6 | Pin32 | GND |  |  |  |
| J6 | Pin33 | SD2\_DATA0 | SD2\_DATA0 | AC28 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin34 | SD2\_WP | SD2\_WP | AC26 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin35 | SD2\_DATA1 | SD2\_DATA1 | AC29 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin36 | SD2\_nCD | SD2\_CD\_B | AD29 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin37 | SD2\_DATA2 | SD2\_DATA2 | AA26 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin38 | SD2\_CLK | SD2\_CLK | AB29 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin39 | GND |  |  |  |
| J6 | Pin40 | SD2\_CMD | SD2\_CMD | AB28 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin41 | QSPIA\_SCLK | NAND\_ALE | N25 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin42 | SD2\_DATA3 | SD2\_DATA3 | AA25 | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin43 | PMIC\_32K\_OUT |  |  |  |
| J6 | Pin44 | QSPIA\_nSS0 | NAND\_CE0\_B | L26 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin45 | SYS\_nRST |  |  |  |
| J6 | Pin46 | QSPIA\_DATA0 | NAND\_DATA00 | R25 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin47 | VSD\_3V3 |  |  |  |
| J6 | Pin48 | QSPIA\_DATA1 | NAND\_DATA01 | L25 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin49 | VSD\_3V3 |  |  |  |
| J6 | Pin50 | QSPIA\_DATA2 | NAND\_DATA02 | L24 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin51 | VSD\_3V3 |  |  |  |
| J6 | Pin52 | QSPIA\_DATA3 | NAND\_DATA03 | N24 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin53 | VDD\_3V3 |  |  |  |
| J6 | Pin54 | VDD\_1V8 |  |  |  |
| J6 | Pin55 | VDD\_3V3 |  |  |  |
| J6 | Pin56 | VDD\_1V8 |  |  |  |
| J6 | Pin57 | VDD\_3V3 |  |  |  |
| J6 | Pin58 | VDD\_1V8 |  |  |  |
| J6 | Pin59 | VDD\_3V3 |  |  |  |
| J6 | Pin60 | VDD\_1V8 |  |  |  |
| J6 | Pin61 | GND |  |  |  |
| J6 | Pin62 | GND |  |  |  |
| J6 | Pin63 | GND |  |  |  |
| J6 | Pin64 | GND |  |  |  |
| J6 | Pin65 | GND |  |  |  |
| J6 | Pin66 | GND |  |  |  |
| J6 | Pin67 | GND |  |  |  |
| J6 | Pin68 | GND |  |  |  |
| J6 | Pin69 | GND |  |  |  |
| J6 | Pin70 | GND |  |  |  |
| J6 | Pin71 | VSYS\_5V |  |  |  |
| J6 | Pin72 | VSYS\_5V |  |  |  |
| J6 | Pin73 | VSYS\_5V |  |  |  |
| J6 | Pin74 | VSYS\_5V |  |  |  |
| J6 | Pin75 | VSYS\_5V |  |  |  |
| J6 | Pin76 | VSYS\_5V |  |  |  |
| J6 | Pin77 | VSYS\_5V |  |  |  |
| J6 | Pin78 | VSYS\_5V |  |  |  |
| J6 | Pin79 | VSYS\_5V |  |  |  |
| J6 | Pin80 | VSYS\_5V |  |  |  |

**3.3 Connector Pin multiplexing**

Table headers instructions are as below:

* Default: Functional definition we used(Defined in schematics)
* BALL\_NAME: CPU pin definition of the corresponding pin
* BALL: CPU pin serial number
* ALT\_NAME: alternative function name

**3.3.1 J3 pin multiplex table**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **BALL** | **ALT0/000** | **ALT1/001** | **ALT2/010** | **ALT3/011** | **ALT4/100** | **ALT5/101** | **ALT6/110** | **NOTES** |
| J3 | Pin1 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin2 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin3 | GPIO1\_IO06 | A3 | GPIO1\_IO06 | ENET\_QOS\_MDC |  | ISP\_SHUTTER\_TRIG\_1 |  | USDHC1\_CD\_B | CCM\_EXT\_CLK3 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin4 | GPIO1\_IO15 | B5 | GPIO1\_IO15 | USB2\_OC |  |  | USDHC3\_WP | PWM4\_OUT | CCM\_CLKO2 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin5 | GPIO1\_IO05 | B4 | GPIO1\_IO05 | M7\_NMI |  | ISP\_FL\_TRIG\_1 |  | CCM\_PMIC\_READY |  | NVCC\_GPIO, 1V8, Output high during reset, input with PU after reset |
| J3 | Pin6 | GPIO1\_IO14 | A4 | GPIO1\_IO14 | USB2\_PWR |  |  | USDHC3\_CD\_B | PWM3\_OUT | CCM\_CLKO1 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin7 | GPIO1\_IO01 | E8 | GPIO1\_IO01 | PWM1\_OUT |  | ISP\_SHUTTER\_TRIG\_0 |  | REF\_CLK\_24M | CCM\_EXT\_CLK2 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset |
| J3 | Pin8 | GPIO1\_IO13 | A6 | GPIO1\_IO13 | USB1\_OC |  |  |  | PWM2\_OUT |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin9 | GPIO1\_IO00 | A7 | GPIO1\_IO00 | CCM\_ENET\_PHY\_REF\_CLK\_ROOT |  | ISP\_FL\_TRIG\_0 |  | REF\_CLK\_32K | CCM\_EXT\_CLK1 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin10 | GPIO1\_IO12 | A5 | GPIO1\_IO12 | USB1\_PWR |  |  |  | SDMA2\_EXT\_EVENT01 |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin11 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin12 | GPIO1\_IO11 | D8 | GPIO1\_IO11 | USB2\_ID | PWM2\_OUT |  | USDHC3\_VSELECT | CCM\_PMIC\_READY |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin13 | USB1\_RXN | B9 | USB1\_RX\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin14 | GPIO1\_IO10 | B7 | GPIO1\_IO10 | USB1\_ID | PWM3\_OUT |  |  |  |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin15 | USB1\_RXP | A9 | USB1\_RX\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin16 | GPIO1\_IO09 | B8 | GPIO1\_IO09 | ENET\_QOS\_1588\_EVENT0\_OUT | PWM2\_OUT | ISP\_SHUTTER\_OPEN\_1 | USDHC3\_RESET\_B | SDMA2\_EXT\_EVENT00 |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin17 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin18 | GPIO1\_IO08 | A8 | GPIO1\_IO08 | ENET\_QOS\_1588\_EVENT0\_IN | PWM1\_OUT | ISP\_PRELIGHT\_TRIG\_1 | ENET\_QOS\_1588\_EVENT0\_AUX\_IN | USDHC2\_RESET\_B |  | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin19 | USB1\_TXN | B10 | USB1\_TX\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin20 | GPIO1\_IO07 | F6 | GPIO1\_IO07 | ENET\_QOS\_MDIO |  | ISP\_FLASH\_TRIG\_1 |  | USDHC1\_WP | CCM\_EXT\_CLK4 | NVCC\_GPIO, 1V8, Input with PD |
| J3 | Pin21 | USB1\_TXP | A10 | USB1\_TX\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin22 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin23 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin24 | USB1\_DN | E10 | USB1\_D\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin25 | USB2\_RXN | B12 | USB2\_RX\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin26 | USB1\_DP | D10 | USB1\_D\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin27 | USB2\_RXP | A12 | USB2\_RX\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin28 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin29 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin30 | USB2\_DN | E14 | USB2\_D\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin31 | USB2\_TXN | B13 | USB2\_TX\_N |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin32 | USB2\_DP | D14 | USB2\_D\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Input |
| J3 | Pin33 | USB2\_TXP | A13 | USB2\_TX\_P |  |  |  |  |  |  | VDD\_USB\_3P3, 3V3, Output |
| J3 | Pin34 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin35 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin36 | USB1\_VBUS\_3V3 | A11 | USB1\_VBUS |  |  |  |  |  |  | VDD\_USB\_3P3, 3.3V, Input |
| J3 | Pin37 | PCIE\_CLKN | E16 | PCIE\_REF\_PAD\_CLK\_N |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, High-Z |
| J3 | Pin38 | USB2\_VBUS\_3V3 | D12 | USB2\_VBUS |  |  |  |  |  |  | VDD\_USB\_3P3, 3.3V, Input |
| J3 | Pin39 | PCIE\_CLKP | D16 | PCIE\_REF\_PAD\_CLK\_P |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, High-Z |
| J3 | Pin40 | JTAG\_TMS | G14 | JTAG\_TMS |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin41 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin42 | JTAG\_TDO | F14 | JTAG\_TDO |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin43 | PCIE\_RXN | B14 | PCIE\_RXN\_N |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, Input, High-Z |
| J3 | Pin44 | JTAG\_TDI | G16 | JTAG\_TDI |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin45 | PCIE\_RXP | A14 | PCIE\_RXN\_P |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, Input, High-Z |
| J3 | Pin46 | JTAG\_MOD | G20 | JTAG\_MOD |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PD |
| J3 | Pin47 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin48 | JTAG\_TCK | G18 | JTAG\_TCK |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PU |
| J3 | Pin49 | PCIE\_TXN | B15 | PCIE\_TXN\_N |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, Output, High-Z |
| J3 | Pin50 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin51 | PCIE\_TXP | A15 | PCIE\_TXN\_P |  |  |  |  |  |  | VDD\_PCI\_1P8, 1V8, Output, High-Z |
| J3 | Pin52 | CSI1\_DN0 | E18 | MIPI\_CSI1\_D0\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin53 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin54 | CSI1\_DP0 | D18 | MIPI\_CSI1\_D0\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin55 | DSI\_DN0 | B16 | MIPI\_DSI1\_D0\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin56 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin57 | DSI\_DP0 | A16 | MIPI\_DSI1\_D0\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin58 | CSI1\_DN1 | E20 | MIPI\_CSI1\_D1\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin59 | DSI\_DN1 | B17 | MIPI\_DSI1\_D1\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin60 | CSI1\_DP1 | D20 | MIPI\_CSI1\_D1\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin61 | DSI\_DP1 | A17 | MIPI\_DSI1\_D1\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin62 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin63 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin64 | CSI1\_CKN | E22 | MIPI\_CSI1\_CLK\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin65 | DSI\_CKN | B18 | MIPI\_DSI1\_CLK\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin66 | CSI1\_CKP | D22 | MIPI\_CSI1\_CLK\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin67 | DSI\_CKP | A18 | MIPI\_DSI1\_CLK\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin68 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin69 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin70 | CSI1\_DN2 | E24 | MIPI\_CSI1\_D2\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin71 | DSI\_DN2 | B19 | MIPI\_DSI1\_D2\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin72 | CSI1\_DP2 | D24 | MIPI\_CSI1\_D2\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin73 | DSI\_DP2 | A19 | MIPI\_DSI1\_D2\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin74 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin75 | DSI\_DN3 | B20 | MIPI\_DSI1\_D3\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin76 | CSI1\_DN3 | E26 | MIPI\_CSI1\_D3\_N |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin77 | DSI\_DP3 | A20 | MIPI\_DSI1\_D3\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Output low |
| J3 | Pin78 | CSI1\_DP3 | D26 | MIPI\_CSI1\_D3\_P |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J3 | Pin79 | GND |  |  |  |  |  |  |  |  |  |
| J3 | Pin80 | GND |  |  |  |  |  |  |  |  |  |

**3.3.2 J4 pin multiplex table**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **BALL** | **ALT0/000** | **ALT1/001** | **ALT2/010** | **ALT3/011** | **ALT4/100** | **ALT5/101** | **ALT6/110** | **ALT7/111** | **NOTES** |
| J4 | Pin1 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin2 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin3 | LVDS1\_TX0\_P | A26 | LVDS1\_D0\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin4 | CSI2\_DN3 | B21 | MIPI\_CSI2\_D3\_N |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin5 | LVDS1\_TX0\_N | B26 | LVDS1\_D0\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin6 | CSI2\_DP3 | A21 | MIPI\_CSI2\_D3\_P |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin7 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin8 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin9 | LVDS1\_TX1\_P | A27 | LVDS1\_D1\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin10 | CSI2\_DN2 | B22 | MIPI\_CSI2\_D2\_N |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin11 | LVDS1\_TX1\_N | B27 | LVDS1\_D1\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin12 | CSI2\_DP2 | A22 | MIPI\_CSI2\_D2\_P |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin13 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin14 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin15 | LVDS1\_CLK\_P | A28 | LVDS1\_CLK\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin16 | CSI2\_CKN | B23 | MIPI\_CSI2\_CLK\_N |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin17 | LVDS1\_CLK\_N | B28 | LVDS1\_CLK\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin18 | CSI2\_CKP | A23 | MIPI\_CSI2\_CLK\_P |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin19 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin20 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin21 | LVDS1\_TX2\_P | B29 | LVDS1\_D2\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin22 | CSI2\_DN1 | B24 | MIPI\_CSI2\_D1\_N |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin23 | LVDS1\_TX2\_N | C28 | LVDS1\_D2\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin24 | CSI2\_DP1 | A24 | MIPI\_CSI2\_D1\_P |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin25 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin26 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin27 | LVDS1\_TX3\_P | C29 | LVDS1\_D3\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin28 | CSI2\_DN0 | B25 | MIPI\_CSI2\_D0\_N |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin29 | LVDS1\_TX3\_N | D28 | LVDS1\_D3\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin30 | CSI2\_DP0 | A25 | MIPI\_CSI2\_D0\_P |  |  |  |  |  |  |  | VDD\_MIPI\_1P8, 1V8, Input |
| J4 | Pin31 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin32 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin33 | LVDS0\_TX0\_P | D29 | LVDS0\_D0\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin34 | NAND\_DQS | R26 | NAND\_DQS | FLEXSPI\_A\_DQS | AUDIOMIX\_SAI3\_MCLK | ISP\_SHUTTER\_OPEN\_0 | I2C3\_SCL | GPIO3\_IO14 | CORESIGHT\_TRACE12 |  | NVCC\_NAND, 1V8, Input with PD |
| J4 | Pin35 | LVDS0\_TX0\_N | E28 | LVDS0\_D0\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin36 | ONOFF | G22 | ONOFF |  |  |  |  |  |  |  | NVCC\_SNVS, 1V8, Input with PU |
| J4 | Pin37 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin38 | POR\_B | J29 | POR\_B |  |  |  |  |  |  |  | NVCC\_SNVS, 1V8, Input with PU |
| J4 | Pin39 | LVDS0\_TX1\_P | E29 | LVDS0\_D1\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin40 | PMIC\_ON\_REQ | F22 | PMIC\_ON\_REQ |  |  |  |  |  |  |  | NVCC\_SNVS, 1V8, Output high with PU |
| J4 | Pin41 | LVDS0\_TX1\_N | F28 | LVDS0\_D1\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin42 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin43 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin44 | BOOT\_MODE0 | G10 | BOOT\_MODE0 |  |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin45 | LVDS0\_CLK\_P | F29 | LVDS0\_CLK\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin46 | BOOT\_MODE1 | F8 | BOOT\_MODE1 |  |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin47 | LVDS0\_CLK\_N | G28 | LVDS0\_CLK\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin48 | BOOT\_MODE2 | G8 | BOOT\_MODE2 |  |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin49 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin50 | BOOT\_MODE3 | G12 | BOOT\_MODE3 |  |  |  |  |  |  |  | NVCC\_JTAG, 1V8, Input with PD |
| J4 | Pin51 | LVDS0\_TX2\_P | G29 | LVDS0\_D2\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin52 | WDOG\_B | B6 | GPIO1\_IO02 | WDOG1\_WDOG\_B |  | ISP\_FLASH\_TRIG\_0 |  | WDOG1\_WDOG\_ANY |  | SJC\_DE\_B | NVCC\_GPIO, 1V8, Input with PU |
| J4 | Pin53 | LVDS0\_TX2\_N | H28 | LVDS0\_D2\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin54 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin55 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin56 | CLKIN1 | K28 |  |  |  |  |  |  |  |  | NVCC\_CLK, 1V8, Input with PD |
| J4 | Pin57 | LVDS0\_TX3\_P | H29 | LVDS0\_D3\_P |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin58 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin59 | LVDS0\_TX3\_N | J28 | LVDS0\_D3\_N |  |  |  |  |  |  |  | VDD\_LVDS\_1P8, 1V8 |
| J4 | Pin60 | CLKOUT1 | K29 |  |  |  |  |  |  |  |  | NVCC\_CLK, 1V8, Output low |
| J4 | Pin61 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin62 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin63 | SD1\_STROBE | W26 | USDHC1\_STROBE |  |  | I2C3\_SDA | UART3\_CTS\_B | GPIO2\_IO11 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin64 | CLKIN2 | L28 |  |  |  |  |  |  |  |  | NVCC\_CLK, 1V8, Input with PD |
| J4 | Pin65 | SD1\_RESET\_B | W25 | USDHC1\_RESET\_B | ENET1\_TX\_CLK |  | I2C3\_SCL | UART3\_RTS\_B | GPIO2\_IO10 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin66 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin67 | SD1\_CLK | W28 | USDHC1\_CLK | ENET1\_MDC |  | I2C5\_SCL | UART1\_TX | GPIO2\_IO00 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin68 | CLKOUT2 | L29 |  |  |  |  |  |  |  |  | NVCC\_CLK, 1V8, Output low |
| J4 | Pin69 | SD1\_CMD | W29 | USDHC1\_CMD | ENET1\_MDIO |  | I2C5\_SDA | UART1\_RX | GPIO2\_IO01 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin70 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin71 | SD1\_DATA0 | Y29 | USDHC1\_DATA0 | ENET1\_RGMII\_TD1 |  | I2C6\_SCL | UART1\_RTS\_B | GPIO2\_IO02 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin72 | SD1\_DATA4 | U26 | USDHC1\_DATA4 | ENET1\_RGMII\_TX\_CTL |  | I2C1\_SCL | UART2\_RTS\_B | GPIO2\_IO06 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin73 | SD1\_DATA1 | Y28 | USDHC1\_DATA1 | ENET1\_RGMII\_TD0 |  | I2C6\_SDA | UART1\_CTS\_B | GPIO2\_IO03 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin74 | SD1\_DATA5 | AA29 | USDHC1\_DATA5 | ENET1\_TX\_ER |  | I2C1\_SDA | UART2\_CTS\_B | GPIO2\_IO07 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin75 | SD1\_DATA2 | V29 | USDHC1\_DATA2 | ENET1\_RGMII\_RD0 |  | I2C4\_SCL | UART2\_TX | GPIO2\_IO04 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin76 | SD1\_DATA6 | AA28 | USDHC1\_DATA6 | ENET1\_RGMII\_RX\_CTL |  | I2C2\_SCL | UART3\_TX | GPIO2\_IO08 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin77 | SD1\_DATA3 | V28 | USDHC1\_DATA3 | ENET1\_RGMII\_RD1 |  | I2C4\_SDA | UART2\_RX | GPIO2\_IO05 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin78 | SD1\_DATA7 | U25 | USDHC1\_DATA7 | ENET1\_RX\_ER |  | I2C2\_SDA | UART3\_RX | GPIO2\_IO09 |  |  | NVCC\_SD1, 1V8, Input with PD |
| J4 | Pin79 | GND |  |  |  |  |  |  |  |  |  |  |
| J4 | Pin80 | GND |  |  |  |  |  |  |  |  |  |  |

**3.3.3 J5 pin multiplex table**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **BALL** | **ALT0/000** | **ALT1/001** | **ALT2/010** | **ALT3/011** | **ALT4/100** | **ALT5/101** | **ALT6/110** | **NOTES** |
| J5 | Pin1 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin2 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin3 | I2C2\_SCL | AH6 | I2C2\_SCL | ENET\_QOS\_1588\_EVENT1\_IN | USDHC3\_CD\_B | ECSPI1\_MISO | ENET\_QOS\_1588\_EVENT1\_AUX\_IN | GPIO5\_IO16 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin4 | UART1\_TXD | AJ3 | UART1\_TX | ECSPI3\_MOSI |  |  |  | GPIO5\_IO23 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin5 | I2C2\_SDA | AE8 | I2C2\_SDA | ENET\_QOS\_1588\_EVENT1\_OUT | USDHC3\_WP | ECSPI1\_SS0 |  | GPIO5\_IO17 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin6 | UART1\_RXD | AD6 | UART1\_RX | ECSPI3\_SCLK |  |  |  | GPIO5\_IO22 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin7 | I2C3\_SCL | AJ7 | I2C3\_SCL | PWM4\_OUT | GPT2\_CLK | ECSPI2\_SCLK |  | GPIO5\_IO18 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin8 | UART1\_CTS | AE6 | UART3\_RX | UART1\_CTS\_B | USDHC3\_RESET\_B | GPT1\_CAPTURE2 | CAN2\_TX | GPIO5\_IO26 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin9 | I2C3\_SDA | AJ6 | I2C3\_SDA | PWM3\_OUT | GPT3\_CLK | ECSPI2\_MOSI |  | GPIO5\_IO19 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin10 | UART1\_RTS | AJ4 | UART3\_TX | UART1\_RTS\_B | USDHC3\_VSELECT | GPT1\_CLK | CAN2\_RX | GPIO5\_IO27 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin11 | I2C4\_SCL | AF8 | I2C4\_SCL | PWM2\_OUT | PCIE\_CLKREQ\_B | ECSPI2\_MISO |  | GPIO5\_IO20 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin12 | UART2\_TXD | AH4 | UART2\_TX | ECSPI3\_SS0 |  | GPT1\_COMPARE2 |  | GPIO5\_IO25 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin13 | I2C4\_SDA | AD8 | I2C4\_SDA | PWM1\_OUT |  | ECSPI2\_SS0 |  | GPIO5\_IO21 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin14 | UART2\_RXD | AF6 | UART2\_RX | ECSPI3\_MISO |  | GPT1\_COMPARE3 |  | GPIO5\_IO24 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin15 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin16 | UART4\_TXD | AH5 | UART4\_TX | UART2\_RTS\_B |  | GPT1\_CAPTURE1 | I2C6\_SDA | GPIO5\_IO29 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin17 | SAI1\_TXC | AJ12 | AUDIOMIX\_SAI1\_TX\_BCLK |  |  |  | ENET1\_RGMII\_RXC | GPIO4\_IO11 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin18 | UART4\_RXD | AJ5 | UART4\_RX | UART2\_CTS\_B | PCIE\_CLKREQ\_B | GPT1\_COMPARE1 | I2C6\_SCL | GPIO5\_IO28 |  | NVCC\_I2C\_UART, 1V8, Input with PD |
| J5 | Pin19 | SAI1\_TXD0 | AJ11 | AUDIOMIX\_SAI1\_TX\_DATA00 |  |  |  | ENET1\_RGMII\_TD0 | GPIO4\_IO12 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin20 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin21 | SAI1\_TXD1 | AJ10 | AUDIOMIX\_SAI1\_TX\_DATA01 |  |  |  | ENET1\_RGMII\_TD1 | GPIO4\_IO13 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin22 | SAI1\_RXFS | AJ9 | AUDIOMIX\_SAI1\_RX\_SYNC |  |  |  | ENET1\_1588\_EVENT0\_IN | GPIO4\_IO00 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin23 | SAI1\_TXD2 | AH11 | AUDIOMIX\_SAI1\_TX\_DATA02 |  |  |  | ENET1\_RGMII\_TD2 | GPIO4\_IO14 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin24 | SAI1\_RXC | AH8 | AUDIOMIX\_SAI1\_RX\_BCLK |  |  | AUDIOMIX\_PDM\_CLK | ENET1\_1588\_EVENT0\_OUT | GPIO4\_IO01 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin25 | SAI1\_TXD3 | AD12 | AUDIOMIX\_SAI1\_TX\_DATA03 |  |  |  | ENET1\_RGMII\_TD3 | GPIO4\_IO15 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin26 | SAI1\_RXD0 | AC10 | AUDIOMIX\_SAI1\_RX\_DATA00 |  | AUDIOMIX\_SAI1\_TX\_DATA01 | AUDIOMIX\_PDM\_BIT\_STREAM00 | ENET1\_1588\_EVENT1\_IN | GPIO4\_IO02 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin27 | SAI1\_TXD4 | AH13 | AUDIOMIX\_SAI1\_TX\_DATA04 | AUDIOMIX\_SAI6\_RX\_BCLK | AUDIOMIX\_SAI6\_TX\_BCLK |  | ENET1\_RGMII\_TX\_CTL | GPIO4\_IO16 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin28 | SAI1\_RXD1 | AF10 | AUDIOMIX\_SAI1\_RX\_DATA01 |  |  | AUDIOMIX\_PDM\_BIT\_STREAM01 | ENET1\_1588\_EVENT1\_OUT | GPIO4\_IO03 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin29 | SAI1\_TXD5 | AH14 | AUDIOMIX\_SAI1\_TX\_DATA05 | AUDIOMIX\_SAI6\_RX\_DATA00 | AUDIOMIX\_SAI6\_TX\_DATA00 |  | ENET1\_RGMII\_TXC | GPIO4\_IO17 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin30 | SAI1\_RXD2 | AH9 | AUDIOMIX\_SAI1\_RX\_DATA02 |  |  | AUDIOMIX\_PDM\_BIT\_STREAM02 | ENET1\_MDC | GPIO4\_IO04 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin31 | SAI1\_TXD6 | AC12 | AUDIOMIX\_SAI1\_TX\_DATA06 | AUDIOMIX\_SAI6\_RX\_SYNC | AUDIOMIX\_SAI6\_TX\_SYNC |  | ENET1\_RX\_ER | GPIO4\_IO18 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin32 | SAI1\_RXD3 | AJ8 | AUDIOMIX\_SAI1\_RX\_DATA03 |  |  | AUDIOMIX\_PDM\_BIT\_STREAM03 | ENET1\_MDIO | GPIO4\_IO05 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin33 | SAI1\_TXD7 | AJ13 | AUDIOMIX\_SAI1\_TX\_DATA07 | AUDIOMIX\_SAI6\_MCLK | AUDIOMIX\_PDM\_CLK | AUDIOMIX\_PDM\_CLK | ENET1\_TX\_ER | GPIO4\_IO19 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin34 | SAI1\_RXD4 | AD10 | AUDIOMIX\_SAI1\_RX\_DATA04 | AUDIOMIX\_SAI6\_TX\_BCLK | AUDIOMIX\_SAI6\_RX\_BCLK |  | ENET1\_RGMII\_RD0 | GPIO4\_IO06 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin35 | SAI1\_TXFS | AF12 | UDIOMIX\_SAI1\_TX\_SYNC |  |  |  | ENET1\_RGMII\_RX\_CTL | GPIO4\_IO10 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin36 | SAI1\_RXD5 | AE10 | AUDIOMIX\_SAI1\_RX\_DATA05 | AUDIOMIX\_SAI6\_TX\_DATA00 | AUDIOMIX\_SAI6\_RX\_DATA00 | AUDIOMIX\_SAI1\_RX\_SYNC | ENET1\_RGMII\_RD1 | GPIO4\_IO07 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin37 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin38 | SAI1\_RXD6 | AH10 | AUDIOMIX\_SAI1\_RX\_DATA06 | AUDIOMIX\_SAI6\_TX\_SYNC | AUDIOMIX\_SAI6\_RX\_SYNC |  | ENET1\_RGMII\_RD2 | GPIO4\_IO08 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin39 | SAI5\_RXD0 | AE16 | AUDIOMIX\_SAI5\_RX\_DATA00 | AUDIOMIX\_SAI1\_TX\_DATA02 | PWM2\_OUT | I2C5\_SCL | AUDIOMIX\_PDM\_BIT\_STREAM00 | GPIO3\_IO21 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin40 | SAI1\_RXD7 | AH12 | AUDIOMIX\_SAI1\_RX\_DATA07 | AUDIOMIX\_SAI6\_MCLK | AUDIOMIX\_SAI1\_TX\_SYNC | AUDIOMIX\_SAI1\_TX\_DATA04 | ENET1\_RGMII\_RD3 | GPIO4\_IO09 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin41 | SAI5\_RXD1 | AD16 | AUDIOMIX\_SAI5\_RX\_DATA01 | AUDIOMIX\_SAI1\_TX\_DATA03 | AUDIOMIX\_SAI1\_TX\_SYNC | AUDIOMIX\_SAI5\_TX\_SYNC | AUDIOMIX\_PDM\_BIT\_STREAM01 | GPIO3\_IO22 | CAN1\_TX | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin42 | SAI1\_MCLK | AE12 | AUDIOMIX\_SAI1\_MCLK |  | AUDIOMIX\_SAI1\_TX\_BCLK |  | ENET1\_TX\_CLK | GPIO4\_IO20 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin43 | SAI5\_RXD2 | AF16 | AUDIOMIX\_SAI5\_RX\_DATA02 | AUDIOMIX\_SAI1\_TX\_DATA04 | AUDIOMIX\_SAI1\_TX\_SYNC | AUDIOMIX\_SAI5\_TX\_BCLK | AUDIOMIX\_PDM\_BIT\_STREAM02 | GPIO3\_IO23 | CAN1\_RX | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin44 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin45 | SAI5\_RXD3 | AE14 | AUDIOMIX\_SAI5\_RX\_DATA03 | AUDIOMIX\_SAI1\_TX\_DATA05 | AUDIOMIX\_SAI1\_TX\_SYNC | AUDIOMIX\_SAI5\_TX\_DATA00 | AUDIOMIX\_PDM\_BIT\_STREAM03 | GPIO3\_IO24 | CAN2\_TX | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin46 | SAI5\_RXFS | AC14 | AUDIOMIX\_SAI5\_RX\_SYNC | AUDIOMIX\_SAI1\_TX\_DATA00 | PWM4\_OUT | I2C6\_SCL |  | GPIO3\_IO19 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin47 | SAI2\_TXC | AH15 | AUDIOMIX\_SAI2\_TX\_BCLK | AUDIOMIX\_SAI5\_TX\_DATA02 |  | CAN1\_RX |  | GPIO4\_IO25 | AUDIOMIX\_PDM\_BIT\_STREAM01 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin48 | SAI5\_RXC | AD14 | AUDIOMIX\_SAI5\_RX\_BCLK | AUDIOMIX\_SAI1\_TX\_DATA01 | PWM3\_OUT | I2C6\_SDA | AUDIOMIX\_PDM\_CLK | GPIO3\_IO20 |  | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin49 | SAI2\_TXFS | AJ17 | AUDIOMIX\_SAI2\_TX\_SYNC | AUDIOMIX\_SAI5\_TX\_DATA01 | ENET\_QOS\_1588\_EVENT3\_OUT | AUDIOMIX\_SAI2\_TX\_DATA01 | UART1\_CTS\_B | GPIO4\_IO24 | AUDIOMIX\_PDM\_BIT\_STREAM02 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin50 | SAI5\_MCLK | AF14 | AUDIOMIX\_SAI5\_MCLK | AUDIOMIX\_SAI1\_TX\_BCLK | PWM1\_OUT | I2C5\_SDA |  | GPIO3\_IO25 | CAN2\_RX | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin51 | SAI2\_TXD | AH16 | AUDIOMIX\_SAI2\_TX\_DATA00 | AUDIOMIX\_SAI5\_TX\_DATA03 | ENET\_QOS\_1588\_EVENT2\_IN | CAN2\_TX | ENET\_QOS\_1588\_EVENT2\_AUX\_IN | GPIO4\_IO26 |  | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin52 | SAI2\_RXFS | AH17 | AUDIOMIX\_SAI2\_RX\_SYNC | AUDIOMIX\_SAI5\_TX\_SYNC | AUDIOMIX\_SAI5\_TX\_DATA01 | AUDIOMIX\_SAI2\_RX\_DATA01 | UART1\_TX | GPIO4\_IO21 | AUDIOMIX\_PDM\_BIT\_STREAM02 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin53 | SAI2\_RXD | AJ14 | AUDIOMIX\_SAI2\_RX\_DATA00 | AUDIOMIX\_SAI5\_TX\_DATA00 | ENET\_QOS\_1588\_EVENT2\_OUT | AUDIOMIX\_SAI2\_TX\_DATA01 | UART1\_RTS\_B | GPIO4\_IO23 | AUDIOMIX\_PDM\_BIT\_STREAM03 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin54 | SAI2\_RXC | AJ16 | AUDIOMIX\_SAI2\_RX\_BCLK | AUDIOMIX\_SAI5\_TX\_BCLK |  | CAN1\_TX | UART1\_RX | GPIO4\_IO22 | AUDIOMIX\_PDM\_BIT\_STREAM01 | NVCC\_SAI1\_SAI5, 1V8, Input with PD |
| J5 | Pin55 | SAI3\_TXC | AH19 | AUDIOMIX\_SAI3\_TX\_BCLK | AUDIOMIX\_SAI2\_TX\_DATA02 | AUDIOMIX\_SAI5\_RX\_DATA02 | GPT1\_CAPTURE1 | UART2\_TX | GPIO5\_IO00 | AUDIOMIX\_PDM\_BIT\_STREAM02 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin56 | SAI2\_MCLK | AJ15 | AUDIOMIX\_SAI2\_MCLK | AUDIOMIX\_SAI5\_MCLK | ENET\_QOS\_1588\_EVENT3\_IN | CAN2\_RX | ENET\_QOS\_1588\_EVENT3\_AUX\_IN | GPIO4\_IO27 | AUDIOMIX\_SAI3\_MCLK | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin57 | SAI3\_TXFS | AC16 | AUDIOMIX\_SAI3\_TX\_SYNC | AUDIOMIX\_SAI2\_TX\_DATA01 | AUDIOMIX\_SAI5\_RX\_DATA01 | AUDIOMIX\_SAI3\_TX\_DATA01 | UART2\_RX | GPIO4\_IO31 | AUDIOMIX\_PDM\_BIT\_STREAM03 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin58 | SAI3\_MCLK | AJ20 | AUDIOMIX\_SAI3\_MCLK | PWM4\_OUT | AUDIOMIX\_SAI5\_MCLK |  | AUDIOMIX\_SPDIF1\_OUT | GPIO5\_IO02 | AUDIOMIX\_SPDIF1\_IN | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin59 | SAI3\_TXD | AH18 | AUDIOMIX\_SAI3\_TX\_DATA00 | AUDIOMIX\_SAI2\_TX\_DATA03 | AUDIOMIX\_SAI5\_RX\_DATA03 | GPT1\_CAPTURE2 | AUDIOMIX\_SPDIF1\_EXT\_CLK | GPIO5\_IO01 |  | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin60 | SAI3\_RXC | AJ18 | AUDIOMIX\_SAI3\_RX\_BCLK | AUDIOMIX\_SAI2\_RX\_DATA02 | AUDIOMIX\_SAI5\_RX\_BCLK | GPT1\_CLK | UART2\_CTS\_B | GPIO4\_IO29 | AUDIOMIX\_PDM\_CLK | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin61 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin62 | SAI3\_RXFS | AJ19 | AUDIOMIX\_SAI3\_RX\_SYNC | AUDIOMIX\_SAI2\_RX\_DATA01 | AUDIOMIX\_SAI5\_RX\_SYNC | AUDIOMIX\_SAI3\_RX\_DATA01 | AUDIOMIX\_SPDIF1\_IN | GPIO4\_IO28 | AUDIOMIX\_PDM\_BIT\_STREAM00 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin63 | ECSPI2\_SCLK | AH21 | ECSPI2\_SCLK | UART4\_RX | I2C3\_SCL | AUDIOMIX\_SAI7\_TX\_BCLK |  | GPIO5\_IO10 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin64 | SAI3\_RXD | AF18 | AUDIOMIX\_SAI3\_RX\_DATA00 | AUDIOMIX\_SAI2\_RX\_DATA03 | AUDIOMIX\_SAI5\_RX\_DATA00 |  | UART2\_RTS\_B | GPIO4\_IO30 | AUDIOMIX\_PDM\_BIT\_STREAM01 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin65 | ECSPI2\_SS0 | AJ22 | ECSPI2\_SS0 | UART4\_RTS\_B | I2C4\_SDA |  | CCM\_CLKO2 | GPIO5\_IO13 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin66 | SPDIF\_TX | AE18 | AUDIOMIX\_SPDIF1\_OUT | PWM3\_OUT | I2C5\_SCL | GPT1\_COMPARE1 | CAN1\_TX | GPIO5\_IO03 |  | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin67 | ECSPI2\_MOSI | AJ21 | ECSPI2\_MOSI | UART4\_TX | I2C3\_SDA | AUDIOMIX\_SAI7\_TX\_DATA00 |  | GPIO5\_IO11 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin68 | SPDIF\_RX | AD18 | AUDIOMIX\_SPDIF1\_IN | PWM2\_OUT | I2C5\_SDA | GPT1\_COMPARE2 | CAN1\_RX | GPIO5\_IO04 |  | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin69 | ECSPI2\_MISO | AH20 | ECSPI2\_MISO | UART4\_CTS\_B | I2C4\_SCL | AUDIOMIX\_SAI7\_MCLK | CCM\_CLKO1 | GPIO5\_IO12 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin70 | SPDIF\_EXT\_CLK | AC18 | AUDIOMIX\_SPDIF1\_EXT\_CLK | PWM1\_OUT |  | GPT1\_COMPARE3 |  | GPIO5\_IO05 |  | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD |
| J5 | Pin71 | HDMI\_DDC\_SCL | AC22 | HDMIMIX\_HDMI\_SCL |  |  | I2C5\_SCL | CAN1\_TX | GPIO3\_IO26 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin72 | UART3\_CTS | AD20 | ECSPI1\_MISO | UART3\_CTS\_B | I2C2\_SCL | AUDIOMIX\_SAI7\_RX\_DATA00 |  | GPIO5\_IO08 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin73 | HDMI\_DDC\_SDA | AF22 | HDMIMIX\_HDMI\_SDA |  |  | I2C5\_SDA | CAN1\_RX | GPIO3\_IO27 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin74 | UART3\_RTS | AE20 | ECSPI1\_SS0 | UART3\_RTS\_B | I2C2\_SDA | AUDIOMIX\_SAI7\_TX\_SYNC |  | GPIO5\_IO09 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin75 | HDMI\_HPD | AE22 | HDMIMIX\_HDMI\_HPD | AUDIOMIX\_HDMI\_HPD\_O |  | I2C6\_SDA | CAN2\_RX | GPIO3\_IO29 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin76 | UART3\_TXD | AC20 | ECSPI1\_MOSI | UART3\_TX | I2C1\_SDA | AUDIOMIX\_SAI7\_RX\_BCLK |  | GPIO5\_IO07 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin77 | HDMI\_CEC | AD22 | HDMIMIX\_HDMI\_CEC |  |  | I2C6\_SCL | CAN2\_TX | GPIO3\_IO28 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin78 | UART3\_RXD | AF20 | ECSPI1\_SCLK | UART3\_RX | I2C1\_SCL | AUDIOMIX\_SAI7\_RX\_SYNC |  | GPIO5\_IO06 |  | NVCC\_ECSPI\_HDMI, 1V8, Input with PD |
| J5 | Pin79 | GND |  |  |  |  |  |  |  |  |  |
| J5 | Pin80 | GND |  |  |  |  |  |  |  |  |  |

**3.3.4 J6 pin multiplex table**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **BALL** | **ALT0/000** | **ALT1/001** | **ALT2/010** | **ALT3/011** | **ALT4/100** | **ALT5/101** | **ALT6/110** | **NOTES** |
| J6 | Pin1 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin2 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin3 | EARC\_N\_HPD | AH22 | EARC\_N\_HPD |  |  |  |  |  |  | VDD\_EARC\_1P8, 1V8, Output |
| J6 | Pin4 | ENET\_MDC | AH28 | ENET\_QOS\_MDC |  | AUDIOMIX\_SAI6\_TX\_DATA00 |  |  | GPIO1\_IO16 | USDHC3\_STROBE | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin5 | EARC\_P\_UTIL | AJ23 | EARC\_P\_UTIL |  |  |  |  |  |  | VDD\_EARC\_1P8, 1V8, Output |
| J6 | Pin6 | ENET\_MDIO | AH29 | ENET\_QOS\_MDIO |  | AUDIOMIX\_SAI6\_TX\_SYNC | AUDIOMIX\_PDM\_BIT\_STREAM03 |  | GPIO1\_IO17 | USDHC3\_DATA5 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin7 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin8 | ENET\_TX\_CTL | AF24 | ENET\_QOS\_RGMII\_TX\_CTL |  | AUDIOMIX\_SAI6\_MCLK | AUDIOMIX\_SPDIF1\_OUT |  | GPIO1\_IO22 | USDHC3\_DATA0 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin9 | HDMI\_TXCN | AJ24 | HDMI\_TXC\_N |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin10 | ENET\_TXC | AE24 | CCM\_ENET\_QOS\_CLOCK\_GENERATE\_TX\_CLK | ENET\_QOS\_TX\_ER | AUDIOMIX\_SAI7\_TX\_DATA00 |  |  | GPIO1\_IO23 | USDHC3\_DATA1 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin11 | HDMI\_TXCP | AH24 | HDMI\_TXC\_P |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin12 | ENET\_TD0 | AC25 | ENET\_QOS\_RGMII\_TD0 |  | AUDIOMIX\_SAI6\_RX\_BCLK | AUDIOMIX\_PDM\_CLK |  | GPIO1\_IO21 | USDHC3\_WP | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin13 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin14 | ENET\_TD1 | AE26 | ENET\_QOS\_RGMII\_TD1 |  | AUDIOMIX\_SAI6\_RX\_SYNC | AUDIOMIX\_PDM\_BIT\_STREAM00 |  | GPIO1\_IO20 | USDHC3\_CD\_B | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin15 | HDMI\_TXN0 | AJ25 | HDMI\_TX0\_N |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin16 | ENET\_TD2 | AF26 | ENET\_QOS\_RGMII\_TD2 | ENET\_QOS\_INPUT=ENET\_QOS\_TX\_CLK, OUTPUT=CCM\_ENET\_QOS\_REF\_CLK\_ROOT | AUDIOMIX\_SAI6\_RX\_DATA00 | AUDIOMIX\_PDM\_BIT\_STREAM01 |  | GPIO1\_IO19 | USDHC3\_DATA7 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin17 | HDMI\_TXP0 | AH25 | HDMI\_TX0\_P |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin18 | ENET\_TD3 | AD24 | ENET\_QOS\_RGMII\_TD3 |  | AUDIOMIX\_SAI6\_TX\_BCLK | AUDIOMIX\_PDM\_BIT\_STREAM02 |  | GPIO1\_IO18 | USDHC3\_DATA6 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin19 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin20 | ENET\_RX\_CTL | AE28 | ENET\_QOS\_RGMII\_RX\_CTL |  | AUDIOMIX\_SAI7\_TX\_SYNC | AUDIOMIX\_PDM\_BIT\_STREAM03 |  | GPIO1\_IO24 | USDHC3\_DATA2 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin21 | HDMI\_TXN1 | AJ26 | HDMI\_TX1\_N |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin22 | ENET\_RXC | AE29 | CCM\_ENET\_QOS\_CLOCK\_GENERATE\_RX\_CLK | ENET\_QOS\_RX\_ER | AUDIOMIX\_SAI7\_TX\_BCLK | AUDIOMIX\_PDM\_BIT\_STREAM02 |  | GPIO1\_IO25 | USDHC3\_DATA3 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin23 | HDMI\_TXP1 | AH26 | HDMI\_TX1\_P |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin24 | ENET\_RD0 | AG29 | ENET\_QOS\_RGMII\_RD0 |  | AUDIOMIX\_SAI7\_RX\_DATA00 | AUDIOMIX\_PDM\_BIT\_STREAM01 |  | GPIO1\_IO26 | USDHC3\_DATA4 | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin25 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin26 | ENET\_RD1 | AG28 | ENET\_QOS\_RGMII\_RD1 |  | AUDIOMIX\_SAI7\_RX\_SYNC | AUDIOMIX\_PDM\_BIT\_STREAM00 |  | GPIO1\_IO27 | USDHC3\_RESET\_B | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin27 | HDMI\_TXN2 | AJ27 | HDMI\_TX2\_N |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin28 | ENET\_RD2 | AF29 | ENET\_QOS\_RGMII\_RD2 |  | AUDIOMIX\_SAI7\_RX\_BCLK | AUDIOMIX\_PDM\_CLK |  | GPIO1\_IO28 | USDHC3\_CLK | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin29 | HDMI\_TXP2 | AH27 | HDMI\_TX2\_P |  |  |  |  |  |  | VDD\_HDMI\_1P8, 1V8 |
| J6 | Pin30 | ENET\_RD3 | AF28 | ENET\_QOS\_RGMII\_RD3 |  | AUDIOMIX\_SAI7\_MCLK | AUDIOMIX\_SPDIF1\_IN |  | GPIO1\_IO29 | USDHC3\_CMD | NVCC\_ENET, 1V8, Input with PD |
| J6 | Pin31 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin32 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin33 | SD2\_DATA0 | AC28 | USDHC2\_DATA0 |  | I2C4\_SDA | UART2\_RX | AUDIOMIX\_PDM\_BIT\_STREAM00 | GPIO2\_IO15 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin34 | SD2\_WP | AC26 | USDHC2\_WP |  |  |  |  | GPIO2\_IO20 | CORESIGHT\_EVENTI | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin35 | SD2\_DATA1 | AC29 | USDHC2\_DATA1 |  | I2C4\_SCL | UART2\_TX | AUDIOMIX\_PDM\_BIT\_STREAM01 | GPIO2\_IO16 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin36 | SD2\_nCD | AD29 | USDHC2\_CD\_B |  |  |  |  | GPIO2\_IO12 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin37 | SD2\_DATA2 | AA26 | USDHC2\_DATA2 |  | ECSPI2\_SS0 | AUDIOMIX\_SPDIF1\_OUT | AUDIOMIX\_PDM\_BIT\_STREAM02 | GPIO2\_IO17 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin38 | SD2\_CLK | AB29 | USDHC2\_CLK |  | ECSPI2\_SCLK | UART4\_RX |  | GPIO2\_IO13 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin39 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin40 | SD2\_CMD | AB28 | USDHC2\_CMD |  | ECSPI2\_MOSI | UART4\_TX | AUDIOMIX\_PDM\_CLK | GPIO2\_IO14 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin41 | QSPIA\_SCLK | N25 | NAND\_ALE | FLEXSPI\_A\_SCLK | AUDIOMIX\_SAI3\_TX\_BCLK | ISP\_FL\_TRIG\_0 | UART3\_RX | GPIO3\_IO00 | CORESIGHT\_TRACE\_CLK | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin42 | SD2\_DATA3 | AA25 | USDHC2\_DATA3 |  | ECSPI2\_MISO | AUDIOMIX\_SPDIF1\_IN | AUDIOMIX\_PDM\_BIT\_STREAM3 | GPIO2\_IO18 |  | NVCC\_SD2, 1V8, Input with PD |
| J6 | Pin43 | PMIC\_32K\_OUT |  |  |  |  |  |  |  |  |  |
| J6 | Pin44 | QSPIA\_nSS0 | L26 | NAND\_CE0\_B | FLEXSPI\_A\_SS0\_B | AUDIOMIX\_SAI3\_TX\_DATA00 | ISP\_SHUTTER\_TRIG\_0 | UART3\_TX | GPIO3\_IO01 | CORESIGHT\_TRACE\_CTL | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin45 | SYS\_nRST |  |  |  |  |  |  |  |  |  |
| J6 | Pin46 | QSPIA\_DATA0 | R25 | NAND\_DATA00 | FLEXSPI\_A\_DATA00 | AUDIOMIX\_SAI3\_RX\_DATA00 | ISP\_FLASH\_TRIG\_0 | UART4\_RX | GPIO3\_IO06 | CORESIGHT\_TRACE04 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin47 | VSD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin48 | QSPIA\_DATA1 | L25 | NAND\_DATA01 | FLEXSPI\_A\_DATA01 | AUDIOMIX\_SAI3\_TX\_SYNC | ISP\_PRELIGHT\_TRIG\_0 | UART4\_TX | GPIO3\_IO07 | CORESIGHT\_TRACE05 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin49 | VSD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin50 | QSPIA\_DATA2 | L24 | NAND\_DATA02 | FLEXSPI\_A\_DATA02 | USDHC3\_CD\_B | UART4\_CTS\_B | I2C4\_SDA | GPIO3\_IO08 | CORESIGHT\_TRACE06 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin51 | VSD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin52 | QSPIA\_DATA3 | N24 | NAND\_DATA03 | FLEXSPI\_A\_DATA03 | USDHC3\_WP | UART4\_RTS\_B | ISP\_FL\_TRIG\_1 | GPIO3\_IO09 | CORESIGHT\_TRACE07 | NVCC\_NAND, 1V8, Input with PD |
| J6 | Pin53 | VDD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin54 | VDD\_1V8 |  |  |  |  |  |  |  |  |  |
| J6 | Pin55 | VDD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin56 | VDD\_1V8 |  |  |  |  |  |  |  |  |  |
| J6 | Pin57 | VDD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin58 | VDD\_1V8 |  |  |  |  |  |  |  |  |  |
| J6 | Pin59 | VDD\_3V3 |  |  |  |  |  |  |  |  |  |
| J6 | Pin60 | VDD\_1V8 |  |  |  |  |  |  |  |  |  |
| J6 | Pin61 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin62 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin63 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin64 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin65 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin66 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin67 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin68 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin69 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin70 | GND |  |  |  |  |  |  |  |  |  |
| J6 | Pin71 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin72 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin73 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin74 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin75 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin76 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin77 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin78 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin79 | VSYS\_5V |  |  |  |  |  |  |  |  |  |
| J6 | Pin80 | VSYS\_5V |  |  |  |  |  |  |  |  |  |

**Chapter 4 Interfaces**

**4.1 Display interfaces**

i.MX 8M Plus SoC supports the following display

Three LCDIF display controller:

* One LCDIF drives MIPI DSI
* One LCDIF dirves LVDS Tx
* One LCDIF drives HDMI Tx

Support up to 1080p60 display per LCDIF if no more than 2 instances are used simultaneously, or 1x1080p60 + 2x720p60 if all 3 instances are used simultaneously

DEBIX SOM A supports all the HDMI, MIPI DSI, LVDS display interfaces that provided by i.MX 8M Plus SoC.

**4.1.1 HDMI**

HDMI 2.0a Tx support one display

* Resolution: 740x480p60, 720x480p60, 1280x720p60, 1920x1080p60,

1920x1080p120, 3840x2160p30

* HDCP is not supported

Audio support

* 32 channel audio output support
* 1 S/PDIF audio eARC input support

HDMI signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ATL#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin77 | HDMI\_CEC | HDMIMIX\_HDMI\_CEC | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD22 | HDMI\_CEC |
| J5 | Pin75 | HDMI\_HPD | HDMIMIX\_HDMI\_HPD | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE22 | HDMI\_HPD |
| J5 | Pin75 | HDMI\_HPD | AUDIOMIX\_HDMI\_HPD\_O | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE22 | HDMI\_HPD |
| J5 | Pin71 | HDMI\_DDC\_SCL | HDMIMIX\_HDMI\_SCL | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC22 | HDMI\_DDC\_SCL |
| J5 | Pin73 | HDMI\_DDC\_SDA | HDMIMIX\_HDMI\_SDA | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF22 | HDMI\_DDC\_SDA |
| J6 | Pin15 | HDMI\_TXN0 | HDMI\_TX0\_N | 0 | VDD\_HDMI\_1P8, 1V8 | AJ25 | HDMI\_TX0\_N |
| J6 | Pin17 | HDMI\_TXP0 | HDMI\_TX0\_P | 0 | VDD\_HDMI\_1P8, 1V8 | AH25 | HDMI\_TX0\_P |
| J6 | Pin21 | HDMI\_TXN1 | HDMI\_TX1\_N | 0 | VDD\_HDMI\_1P8, 1V8 | AJ26 | HDMI\_TX1\_N |
| J6 | Pin23 | HDMI\_TXP1 | HDMI\_TX1\_P | 0 | VDD\_HDMI\_1P8, 1V8 | AH26 | HDMI\_TX1\_P |
| J6 | Pin27 | HDMI\_TXN2 | HDMI\_TX2\_N | 0 | VDD\_HDMI\_1P8, 1V8 | AJ27 | HDMI\_TX2\_N |
| J6 | Pin29 | HDMI\_TXP2 | HDMI\_TX2\_P | 0 | VDD\_HDMI\_1P8, 1V8 | AH27 | HDMI\_TX2\_P |
| J6 | Pin9 | HDMI\_TXCN | HDMI\_TXC\_N | 0 | VDD\_HDMI\_1P8, 1V8 | AJ24 | HDMI\_TXC\_N |
| J6 | Pin11 | HDMI\_TXCP | HDMI\_TXC\_P | 0 | VDD\_HDMI\_1P8, 1V8 | AH24 | HDMI\_TXC\_P |

HDMI eARC signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J6 | Pin5 | EARC\_P\_UTIL | EARC\_P\_UTIL | 0 | VDD\_EARC\_1P8, 1V8, Output | AJ23 | EARC\_P\_UTIL |
| J6 | Pin3 | EARC\_N\_HPD | EARC\_N\_HPD | 0 | VDD\_EARC\_1P8, 1V8, Output | AH22 | EARC\_N\_HPD |

**4.1.2 LVDS**

The LVDS Display Bridge (LDB) connects the CPU internal LCDIF to External LVDS Display.

The purpose of the LDB is to support flow of synchronous RGB data to external display

devices through the LVDS interface.

The LVDS ports can be used as follows:

* Single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock. This supports resolutions up to 1366x768p60.
* Dual asynchronous channels (8 data, 2 clocks). This is intended for a single panel with two interfaces, transferring across two channels (even pixel/odd pixel). This is supported at up to 160MHz pixel clock, which is up to 80MHz LVDS clock (due to 2 pixels per LVDS clock). This supports resolutions above 1366x768p60, up to 1080p60.

The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream. Splitting and reordering is required to match the LVDS Displays speed and channel requirements. Both VESA and JEIDA pixel mapping are supported.

LVDS signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J4 | Pin3 | LVDS1\_TX0\_P | LVDS1\_D0\_P | 0 | VDD\_LVDS\_1P8, 1V8 | A26 | LVDS1\_D0\_P |
| J4 | Pin5 | LVDS1\_TX0\_N | LVDS1\_D0\_N | 0 | VDD\_LVDS\_1P8, 1V8 | B26 | LVDS1\_D0\_N |
| J4 | Pin9 | LVDS1\_TX1\_P | LVDS1\_D1\_P | 0 | VDD\_LVDS\_1P8, 1V8 | A27 | LVDS1\_D1\_P |
| J4 | Pin11 | LVDS1\_TX1\_N | LVDS1\_D1\_N | 0 | VDD\_LVDS\_1P8, 1V8 | B27 | LVDS1\_D1\_N |
| J4 | Pin15 | LVDS1\_CLK\_P | LVDS1\_CLK\_P | 0 | VDD\_LVDS\_1P8, 1V8 | A28 | LVDS1\_CLK\_P |
| J4 | Pin17 | LVDS1\_CLK\_N | LVDS1\_CLK\_N | 0 | VDD\_LVDS\_1P8, 1V8 | B28 | LVDS1\_CLK\_N |
| J4 | Pin21 | LVDS1\_TX2\_P | LVDS1\_D2\_P | 0 | VDD\_LVDS\_1P8, 1V8 | B29 | LVDS1\_D2\_P |
| J4 | Pin23 | LVDS1\_TX2\_N | LVDS1\_D2\_N | 0 | VDD\_LVDS\_1P8, 1V8 | C28 | LVDS1\_D2\_N |
| J4 | Pin27 | LVDS1\_TX3\_P | LVDS1\_D3\_P | 0 | VDD\_LVDS\_1P8, 1V8 | C29 | LVDS1\_D3\_P |
| J4 | Pin29 | LVDS1\_TX3\_N | LVDS1\_D3\_N | 0 | VDD\_LVDS\_1P8, 1V8 | D28 | LVDS1\_D3\_N |
| J4 | Pin33 | LVDS0\_TX0\_P | LVDS0\_D0\_P | 0 | VDD\_LVDS\_1P8, 1V8 | D29 | LVDS0\_D0\_P |
| J4 | Pin35 | LVDS0\_TX0\_N | LVDS0\_D0\_N | 0 | VDD\_LVDS\_1P8, 1V8 | E28 | LVDS0\_D0\_N |
| J4 | Pin39 | LVDS0\_TX1\_P | LVDS0\_D1\_P | 0 | VDD\_LVDS\_1P8, 1V8 | E29 | LVDS0\_D1\_P |
| J4 | Pin41 | LVDS0\_TX1\_N | LVDS0\_D1\_N | 0 | VDD\_LVDS\_1P8, 1V8 | F28 | LVDS0\_D1\_N |
| J4 | Pin45 | LVDS0\_CLK\_P | LVDS0\_CLK\_P | 0 | VDD\_LVDS\_1P8, 1V8 | F29 | LVDS0\_CLK\_P |
| J4 | Pin47 | LVDS0\_CLK\_N | LVDS0\_CLK\_N | 0 | VDD\_LVDS\_1P8, 1V8 | G28 | LVDS0\_CLK\_N |
| J4 | Pin51 | LVDS0\_TX2\_P | LVDS0\_D2\_P | 0 | VDD\_LVDS\_1P8, 1V8 | G29 | LVDS0\_D2\_P |
| J4 | Pin53 | LVDS0\_TX2\_N | LVDS0\_D2\_N | 0 | VDD\_LVDS\_1P8, 1V8 | H28 | LVDS0\_D2\_N |
| J4 | Pin57 | LVDS0\_TX3\_P | LVDS0\_D3\_P | 0 | VDD\_LVDS\_1P8, 1V8 | H29 | LVDS0\_D3\_P |
| J4 | Pin59 | LVDS0\_TX3\_N | LVDS0\_D3\_N | 0 | VDD\_LVDS\_1P8, 1V8 | J28 | LVDS0\_D3\_N |

**4.1.3 DSI**

i.MX 8M Plus incorporates MIPI DSI Host controller

The key features of MIPI DSI includes:

* Complies to MIPI-DSI standard V1.2, be compatible with standard specification V1.01r11
* Maximum resolution ranges up to WQHD (2560x1440), It should be decided on bandwidth between input clock (video clock) and output clock (D-PHY HS clock).
* Supports 1, 2, 3 or 4 data lanes
* Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed(3 bytes format), and 24bpp
* Interfaces
* Complies with Protocol-to-PHY Interface (PPI) in 1.0Gbps / 1.5Gbps MIPI DPHY
* Supports RGB Interface for Video Image Input from general display controller

DSI Signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin55 | DSI\_DN0 | MIPI\_DSI1\_D0\_N | 0 | VDD\_MIPI\_1P8, 1V8, Output low | B16 | MIPI\_DSI1\_D0\_N |
| J3 | Pin57 | DSI\_DP0 | MIPI\_DSI1\_D0\_P | 0 | VDD\_MIPI\_1P8, 1V8, Output low | A16 | MIPI\_DSI1\_D0\_P |
| J3 | Pin59 | DSI\_DN1 | MIPI\_DSI1\_D1\_N | 0 | VDD\_MIPI\_1P8, 1V8, Output low | B17 | MIPI\_DSI1\_D1\_N |
| J3 | Pin61 | DSI\_DP1 | MIPI\_DSI1\_D1\_P | 0 | VDD\_MIPI\_1P8, 1V8, Output low | A17 | MIPI\_DSI1\_D1\_P |
| J3 | Pin65 | DSI\_CKN | MIPI\_DSI1\_CLK\_N | 0 | VDD\_MIPI\_1P8, 1V8, Output low | B18 | MIPI\_DSI1\_CLK\_N |
| J3 | Pin67 | DSI\_CKP | MIPI\_DSI1\_CLK\_P | 0 | VDD\_MIPI\_1P8, 1V8, Output low | A18 | MIPI\_DSI1\_CLK\_P |
| J3 | Pin71 | DSI\_DN2 | MIPI\_DSI1\_D2\_N | 0 | VDD\_MIPI\_1P8, 1V8, Output low | B19 | MIPI\_DSI1\_D2\_N |
| J3 | Pin73 | DSI\_DP2 | MIPI\_DSI1\_D2\_P | 0 | VDD\_MIPI\_1P8, 1V8, Output low | A19 | MIPI\_DSI1\_D2\_P |
| J3 | Pin75 | DSI\_DN3 | MIPI\_DSI1\_D3\_N | 0 | VDD\_MIPI\_1P8, 1V8, Output low | B20 | MIPI\_DSI1\_D3\_N |
| J3 | Pin77 | DSI\_DP3 | MIPI\_DSI1\_D3\_P | 0 | VDD\_MIPI\_1P8, 1V8, Output low | A20 | MIPI\_DSI1\_D3\_P |

**4.2 Camera interface**

**4.2.1 MIPI CSI-2**

DEBIX SOM A has 2 MIPI CSI-2 Host Controller which implements the protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

* Support primary and secondary Image format
* YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
* RGB565, RGB666, RGB888
* RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
* Support up to 4 lanes of D-PHY
* Interfaces
* Image output data buswidth : 32 bits
* Image memory
* Size of SRAM is 4KB
* Pixel clock can be gated when no ppi data is coming

**4.2.1.1 MIPI-CSI2#1 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin64 | CSI1\_CKN | MIPI\_CSI1\_CLK\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | E22 | MIPI\_CSI1\_CLK\_N |
| J3 | Pin66 | CSI1\_CKP | MIPI\_CSI1\_CLK\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | D22 | MIPI\_CSI1\_CLK\_P |
| J3 | Pin52 | CSI1\_DN0 | MIPI\_CSI1\_D0\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | E18 | MIPI\_CSI1\_D0\_N |
| J3 | Pin54 | CSI1\_DP0 | MIPI\_CSI1\_D0\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | D18 | MIPI\_CSI1\_D0\_P |
| J3 | Pin58 | CSI1\_DN1 | MIPI\_CSI1\_D1\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | E20 | MIPI\_CSI1\_D1\_N |
| J3 | Pin60 | CSI1\_DP1 | MIPI\_CSI1\_D1\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | D20 | MIPI\_CSI1\_D1\_P |
| J3 | Pin70 | CSI1\_DN2 | MIPI\_CSI1\_D2\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | E24 | MIPI\_CSI1\_D2\_N |
| J3 | Pin72 | CSI1\_DP2 | MIPI\_CSI1\_D2\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | D24 | MIPI\_CSI1\_D2\_P |
| J3 | Pin76 | CSI1\_DN3 | MIPI\_CSI1\_D3\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | E26 | MIPI\_CSI1\_D3\_N |
| J3 | Pin78 | CSI1\_DP3 | MIPI\_CSI1\_D3\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | D26 | MIPI\_CSI1\_D3\_P |

**4.2.1.2 MIPI-CSI2#2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J4 | Pin16 | CSI2\_CKN | MIPI\_CSI2\_CLK\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | B23 | MIPI\_CSI2\_CLK\_N |
| J4 | Pin18 | CSI2\_CKP | MIPI\_CSI2\_CLK\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | A23 | MIPI\_CSI2\_CLK\_P |
| J4 | Pin28 | CSI2\_DN0 | MIPI\_CSI2\_D0\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | B25 | MIPI\_CSI2\_D0\_N |
| J4 | Pin30 | CSI2\_DP0 | MIPI\_CSI2\_D0\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | A25 | MIPI\_CSI2\_D0\_P |
| J4 | Pin22 | CSI2\_DN1 | MIPI\_CSI2\_D1\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | B24 | MIPI\_CSI2\_D1\_N |
| J4 | Pin24 | CSI2\_DP1 | MIPI\_CSI2\_D1\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | A24 | MIPI\_CSI2\_D1\_P |
| J4 | Pin10 | CSI2\_DN2 | MIPI\_CSI2\_D2\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | B22 | MIPI\_DSI2\_D2\_N |
| J4 | Pin12 | CSI2\_DP2 | MIPI\_CSI2\_D2\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | A22 | MIPI\_DSI2\_D2\_P |
| J4 | Pin4 | CSI2\_DN3 | MIPI\_CSI2\_D3\_N | 0 | VDD\_MIPI\_1P8, 1V8, Input | B21 | MIPI\_CSI2\_D3\_N |
| J4 | Pin6 | CSI2\_DP3 | MIPI\_CSI2\_D3\_P | 0 | VDD\_MIPI\_1P8, 1V8, Input | A21 | MIPI\_CSI2\_D3\_P |

**4.2.2 ISP**

The Image Signal Processors (ISP) receive an image from the camera sensor and converts

it from raw Bayer to YUV so it can be processed by the chip. The ISP also provides additional processing to improve the image quality. Supported image quality processes include:

* HDR to retain image details in high contrast scenes
* Dewarp to correct the image geometry caused by lens distortion (e.g. fisheye lens)
* Image enhancements (e.g. AWB, Denoise, AE, etc)

There are two instances of ISP on the chip and each is connected to separate instances of

MIPI CSI. Both ISP instances support YCbCr420, YCbCR422, RAW8, RAW10, and RAW12 output pixel formats.

**4.2.2.1 High-Dynamic Range(HDR)**

The ISP supports the following HDR generation for high-quality on-the-fly dynamic

range compression (DRC):

* Native HDR Sensor with compand output (max 14 bit compressed input)
* Digital Overlap High-Dynamic Range Sensor (DOL-HDR), staggered HDR

For Native HDR sensors, the multi-exposure stitching is done internally and has line

buffers.

ISP0 & ISP1 Signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **PIN** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin3 | GPIO1\_IO06 | ISP\_SHUTTER\_TRIG\_1 | 3 | NVCC\_GPIO, 1V8, Input with PD | A3 | GPIO1\_IO06 |
| J3 | Pin5 | GPIO1\_IO05 | ISP\_FL\_TRIG\_1 | 3 | NVCC\_GPIO, 1V8, Output high during reset, input with PU after reset | B4 | GPIO1\_IO05 |
| J3 | Pin7 | GPIO1\_IO01 | ISP\_SHUTTER\_TRIG\_0 | 3 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset | E8 | GPIO1\_IO01 |
| J3 | Pin9 | GPIO1\_IO00 | ISP\_FL\_TRIG\_0 | 3 | NVCC\_GPIO, 1V8, Input with PD | A7 | GPIO1\_IO00 |
| J3 | Pin16 | GPIO1\_IO09 | ISP\_SHUTTER\_OPEN\_1 | 3 | NVCC\_GPIO, 1V8, Input with PD | B8 | GPIO1\_IO09 |
| J3 | Pin18 | GPIO1\_IO08 | ISP\_PRELIGHT\_TRIG\_1 | 3 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J3 | Pin20 | GPIO1\_IO07 | ISP\_FLASH\_TRIG\_1 | 3 | NVCC\_GPIO, 1V8, Input with PD | F6 | GPIO1\_IO07 |
| J4 | Pin34 | NAND\_DQS | ISP\_SHUTTER\_OPEN\_0 | 3 | NVCC\_NAND, 1V8, Input with PD | R26 | NAND\_DQS |
| J4 | Pin52 | WDOG\_B | ISP\_FLASH\_TRIG\_0 | 3 | NVCC\_GPIO, 1V8, Input with PU | B6 | GPIO1\_IO02 |
| J6 | Pin41 | QSPIA\_SCLK | ISP\_FL\_TRIG\_0 | 3 | NVCC\_NAND, 1V8, Input with PD | N25 | NAND\_ALE |
| J6 | Pin44 | QSPIA\_nSS0 | ISP\_SHUTTER\_TRIG\_0 | 3 | NVCC\_NAND, 1V8, Input with PD | L26 | NAND\_CE0\_B |
| J6 | Pin46 | QSPIA\_DATA0 | ISP\_FLASH\_TRIG\_0 | 3 | NVCC\_NAND, 1V8, Input with PD | R25 | NAND\_DATA00 |
| J6 | Pin48 | QSPIA\_DATA1 | ISP\_PRELIGHT\_TRIG\_0 | 3 | NVCC\_NAND, 1V8, Input with PD | L25 | NAND\_DATA01 |
| J6 | Pin52 | QSPIA\_DATA3 | ISP\_FL\_TRIG\_1 | 4 | NVCC\_NAND, 1V8, Input with PD | N24 | NAND\_DATA03 |

**4.3 Ethernet interface**

The iMX 8M Plus implements Two Ethernet controllers, both of them are capable of simultaneous operation.

* ENET\_QOS(Ethernet Quality of Service) , Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588
* ENET1, Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

**4.3.1 ENET\_QOS signals**

ENET\_QOS signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin18 | GPIO1\_IO08 | ENET\_QOS\_1588\_EVENT0\_AUX\_IN | 4 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J3 | Pin18 | GPIO1\_IO08 | ENET\_QOS\_1588\_EVENT0\_IN | 1 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J3 | Pin16 | GPIO1\_IO09 | ENET\_QOS\_1588\_EVENT0\_OUT | 1 | NVCC\_GPIO, 1V8, Input with PD | B8 | GPIO1\_IO09 |
| J5 | Pin3 | I2C2\_SCL | ENET\_QOS\_1588\_EVENT1\_AUX\_IN | 4 | NVCC\_I2C\_UART, 1V8, Input with PD | AH6 | I2C2\_SCL |
| J5 | Pin3 | I2C2\_SCL | ENET\_QOS\_1588\_EVENT1\_IN | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AH6 | I2C2\_SCL |
| J5 | Pin5 | I2C2\_SDA | ENET\_QOS\_1588\_EVENT1\_OUT | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AE8 | I2C2\_SDA |
| J5 | Pin51 | SAI2\_TXD | ENET\_QOS\_1588\_EVENT2\_AUX\_IN | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin51 | SAI2\_TXD | ENET\_QOS\_1588\_EVENT2\_IN | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin53 | SAI2\_RXD | ENET\_QOS\_1588\_EVENT2\_OUT | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin56 | SAI2\_MCLK | ENET\_QOS\_1588\_EVENT3\_AUX\_IN | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin56 | SAI2\_MCLK | ENET\_QOS\_1588\_EVENT3\_IN | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin49 | SAI2\_TXFS | ENET\_QOS\_1588\_EVENT3\_OUT | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J6 | Pin16 | ENET\_TD2 | ENET\_QOS\_INPUT=ENET\_QOS\_TX\_CLK, OUTPUT=CCM\_ENET\_QOS\_REF\_CLK\_ROOT | 1 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J6 | Pin4 | ENET\_MDC | ENET\_QOS\_MDC | 0 | NVCC\_ENET, 1V8, Input with PD | AH28 | ENET\_MDC |
| J3 | Pin3 | GPIO1\_IO06 | ENET\_QOS\_MDC | 1 | NVCC\_GPIO, 1V8, Input with PD | A3 | GPIO1\_IO06 |
| J6 | Pin6 | ENET\_MDIO | ENET\_QOS\_MDIO | 0 | NVCC\_ENET, 1V8, Input with PD | AH29 | ENET\_MDIO |
| J3 | Pin20 | GPIO1\_IO07 | ENET\_QOS\_MDIO | 1 | NVCC\_GPIO, 1V8, Input with PD | F6 | GPIO1\_IO07 |
| J6 | Pin24 | ENET\_RD0 | ENET\_QOS\_RGMII\_RD0 | 0 | NVCC\_ENET, 1V8, Input with PD | AG29 | ENET\_RD0 |
| J6 | Pin26 | ENET\_RD1 | ENET\_QOS\_RGMII\_RD1 | 0 | NVCC\_ENET, 1V8, Input with PD | AG28 | ENET\_RD1 |
| J6 | Pin28 | ENET\_RD2 | ENET\_QOS\_RGMII\_RD2 | 0 | NVCC\_ENET, 1V8, Input with PD | AF29 | ENET\_RD2 |
| J6 | Pin30 | ENET\_RD3 | ENET\_QOS\_RGMII\_RD3 | 0 | NVCC\_ENET, 1V8, Input with PD | AF28 | ENET\_RD3 |
| J6 | Pin20 | ENET\_RX\_CTL | ENET\_QOS\_RGMII\_RX\_CTL | 0 | NVCC\_ENET, 1V8, Input with PD | AE28 | ENET\_RX\_CTL |
| J6 | Pin22 | ENET\_RXC | CCM\_ENET\_QOS\_CLOCK\_GENERATE\_RX\_CLK | 0 | NVCC\_ENET, 1V8, Input with PD | AE29 | ENET\_RXC |
| J6 | Pin12 | ENET\_TD0 | ENET\_QOS\_RGMII\_TD0 | 0 | NVCC\_ENET, 1V8, Input with PD | AC25 | ENET\_TD0 |
| J6 | Pin14 | ENET\_TD1 | ENET\_QOS\_RGMII\_TD1 | 0 | NVCC\_ENET, 1V8, Input with PD | AE26 | ENET\_TD1 |
| J6 | Pin16 | ENET\_TD2 | ENET\_QOS\_RGMII\_TD2 | 0 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J6 | Pin18 | ENET\_TD3 | ENET\_QOS\_RGMII\_TD3 | 0 | NVCC\_ENET, 1V8, Input with PD | AD24 | ENET\_TD3 |
| J6 | Pin8 | ENET\_TX\_CTL | ENET\_QOS\_RGMII\_TX\_CTL | 0 | NVCC\_ENET, 1V8, Input with PD | AF24 | ENET\_TX\_CTL |
| J6 | Pin10 | ENET\_TXC | CCM\_ENET\_QOS\_CLOCK\_GENERATE\_TX\_CLK | 0 | NVCC\_ENET, 1V8, Input with PD | AE24 | ENET\_TXC |
| J6 | Pin22 | ENET\_RXC | ENET\_QOS\_RX\_ER | 1 | NVCC\_ENET, 1V8, Input with PD | AE29 | ENET\_RXC |
| J6 | Pin10 | ENET\_TXC | ENET\_QOS\_TX\_ER | 1 | NVCC\_ENET, 1V8, Input with PD | AE24 | ENET\_TXC |

**4.3.2 ENET1**

ENET1 RGMII/RMII interface signals are always exported.

Signals, in conjunction to MDIO signals exported from connectors, can be used to interface

an external Ethernet PHY or Ethernet switch.

**4.3.2.1 ENET1 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J4 | Pin65 | SD1\_RESET\_B | ENET1\_TX\_CLK | 1 | NVCC\_SD1, 1V8, Input with PD | W25 | SD1\_RESET\_B |
| J4 | Pin67 | SD1\_CLK | ENET1\_MDC | 1 | NVCC\_SD1, 1V8, Input with PD | W28 | SD1\_CLK |
| J4 | Pin69 | SD1\_CMD | ENET1\_MDIO | 1 | NVCC\_SD1, 1V8, Input with PD | W29 | SD1\_CMD |
| J4 | Pin71 | SD1\_DATA0 | ENET1\_RGMII\_TD1 | 1 | NVCC\_SD1, 1V8, Input with PD | Y29 | SD1\_DATA0 |
| J4 | Pin72 | SD1\_DATA4 | ENET1\_RGMII\_TX\_CTL | 1 | NVCC\_SD1, 1V8, Input with PD | U26 | SD1\_DATA4 |
| J4 | Pin73 | SD1\_DATA1 | ENET1\_RGMII\_TD0 | 1 | NVCC\_SD1, 1V8, Input with PD | Y28 | SD1\_DATA1 |
| J4 | Pin74 | SD1\_DATA5 | ENET1\_TX\_ER | 1 | NVCC\_SD1, 1V8, Input with PD | AA29 | SD1\_DATA5 |
| J4 | Pin75 | SD1\_DATA2 | ENET1\_RGMII\_RD0 | 1 | NVCC\_SD1, 1V8, Input with PD | V29 | SD1\_DATA2 |
| J4 | Pin76 | SD1\_DATA6 | ENET1\_RGMII\_RX\_CTL | 1 | NVCC\_SD1, 1V8, Input with PD | AA28 | SD1\_DATA6 |
| J4 | Pin77 | SD1\_DATA3 | ENET1\_RGMII\_RD1 | 1 | NVCC\_SD1, 1V8, Input with PD | V28 | SD1\_DATA3 |
| J4 | Pin78 | SD1\_DATA7 | ENET1\_RX\_ER | 1 | NVCC\_SD1, 1V8, Input with PD | U25 | SD1\_DATA7 |
| J5 | Pin17 | SAI1\_TXC | ENET1\_RGMII\_RXC | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ12 | SAI1\_TXC |
| J5 | Pin19 | SAI1\_TXD0 | ENET1\_RGMII\_TD0 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ11 | SAI1\_TXD0 |
| J5 | Pin21 | SAI1\_TXD1 | ENET1\_RGMII\_TD1 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ10 | SAI1\_TXD1 |
| J5 | Pin22 | SAI1\_RXFS | ENET1\_1588\_EVENT0\_IN | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ9 | SAI1\_RXFS |
| J5 | Pin23 | SAI1\_TXD2 | ENET1\_RGMII\_TD2 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH11 | SAI1\_TXD2 |
| J5 | Pin24 | SAI1\_RXC | ENET1\_1588\_EVENT0\_OUT | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH8 | SAI1\_RXC |
| J5 | Pin25 | SAI1\_TXD3 | ENET1\_RGMII\_TD3 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD12 | SAI1\_TXD3 |
| J5 | Pin26 | SAI1\_RXD0 | ENET1\_1588\_EVENT1\_IN | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC10 | SAI1\_RXD0 |
| J5 | Pin27 | SAI1\_TXD4 | ENET1\_RGMII\_TX\_CTL | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH13 | SAI1\_TXD4 |
| J5 | Pin28 | SAI1\_RXD1 | ENET1\_1588\_EVENT1\_OUT | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF10 | SAI1\_RXD1 |
| J5 | Pin29 | SAI1\_TXD5 | ENET1\_RGMII\_TXC | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH14 | SAI1\_TXD5 |
| J5 | Pin30 | SAI1\_RXD2 | ENET1\_MDC | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH9 | SAI1\_RXD2 |
| J5 | Pin31 | SAI1\_TXD6 | ENET1\_RX\_ER | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC12 | SAI1\_TXD6 |
| J5 | Pin32 | SAI1\_RXD3 | ENET1\_MDIO | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ8 | SAI1\_RXD3 |
| J5 | Pin33 | SAI1\_TXD7 | ENET1\_TX\_ER | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ13 | SAI1\_TXD7 |
| J5 | Pin34 | SAI1\_RXD4 | ENET1\_RGMII\_RD0 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD10 | SAI1\_RXD4 |
| J5 | Pin35 | SAI1\_TXFS | ENET1\_RGMII\_RX\_CTL | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF12 | SAI1\_TXFS |
| J5 | Pin36 | SAI1\_RXD5 | ENET1\_RGMII\_RD1 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J5 | Pin38 | SAI1\_RXD6 | ENET1\_RGMII\_RD2 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH10 | SAI1\_RXD6 |
| J5 | Pin40 | SAI1\_RXD7 | ENET1\_RGMII\_RD3 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |
| J5 | Pin42 | SAI1\_MCLK | ENET1\_TX\_CLK | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |

**4.4 Ultra-Secured Digital Host Controller**

DEBIX SOM A exposes uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.

Key features of uSDHC2:

* SD/SDIO standard, up to version 3.0.
* MMC standard, up to version 5.1.
* 1.8 V and 3.3 V operation
* 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
* Up to SDR104 rate

**4.4.1 uSDHC1 signals**

uSDHC controller, uSDHC1 can be used for external Wi-Fi SDIO interface 4-bits

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin3 | GPIO1\_IO06 | USDHC1\_CD\_B | 5 | NVCC\_GPIO, 1V8, Input with PD | A3 | GPIO1\_IO06 |
| J4 | Pin67 | SD1\_CLK | USDHC1\_CLK | 0 | NVCC\_SD1, 1V8, Input with PD | W28 | SD1\_CLK |
| J4 | Pin69 | SD1\_CMD | USDHC1\_CMD | 0 | NVCC\_SD1, 1V8, Input with PD | W29 | SD1\_CMD |
| J4 | Pin71 | SD1\_DATA0 | USDHC1\_DATA0 | 0 | NVCC\_SD1, 1V8, Input with PD | Y29 | SD1\_DATA0 |
| J4 | Pin73 | SD1\_DATA1 | USDHC1\_DATA1 | 0 | NVCC\_SD1, 1V8, Input with PD | Y28 | SD1\_DATA1 |
| J4 | Pin75 | SD1\_DATA2 | USDHC1\_DATA2 | 0 | NVCC\_SD1, 1V8, Input with PD | V29 | SD1\_DATA2 |
| J4 | Pin77 | SD1\_DATA3 | USDHC1\_DATA3 | 0 | NVCC\_SD1, 1V8, Input with PD | V28 | SD1\_DATA3 |
| J4 | Pin72 | SD1\_DATA4 | USDHC1\_DATA4 | 0 | NVCC\_SD1, 1V8, Input with PD | U26 | SD1\_DATA4 |
| J4 | Pin74 | SD1\_DATA5 | USDHC1\_DATA5 | 0 | NVCC\_SD1, 1V8, Input with PD | AA29 | SD1\_DATA5 |
| J4 | Pin76 | SD1\_DATA6 | USDHC1\_DATA6 | 0 | NVCC\_SD1, 1V8, Input with PD | AA28 | SD1\_DATA6 |
| J4 | Pin78 | SD1\_DATA7 | USDHC1\_DATA7 | 0 | NVCC\_SD1, 1V8, Input with PD | U25 | SD1\_DATA7 |
| J4 | Pin65 | SD1\_RESET\_B | USDHC1\_RESET\_B | 0 | NVCC\_SD1, 1V8, Input with PD | W25 | SD1\_RESET\_B |
| J4 | Pin63 | SD1\_STROBE | USDHC1\_STROBE | 0 | NVCC\_SD1, 1V8, Input with PD | W26 | SD1\_STROBE |
| J3 | Pin20 | GPIO1\_IO07 | USDHC1\_WP | 5 | NVCC\_GPIO, 1V8, Input with PD | F6 | GPIO1\_IO07 |

**4.4.2 uSDHC2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **Notes** | **BALL** | **BALL\_NAME** |
| J3 | Pin18 | GPIO1\_IO08 | USDHC2\_RESET\_B | 5 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J6 | Pin33 | SD2\_DATA0 | USDHC2\_DATA0 | 0 | NVCC\_SD2, 1V8, Input with PD | AC28 | SD2\_DATA0 |
| J6 | Pin34 | SD2\_WP | USDHC2\_WP | 0 | NVCC\_SD2, 1V8, Input with PD | AC26 | SD2\_WP |
| J6 | Pin35 | SD2\_DATA1 | USDHC2\_DATA1 | 0 | NVCC\_SD2, 1V8, Input with PD | AC29 | SD2\_DATA1 |
| J6 | Pin36 | SD2\_nCD | USDHC2\_CD\_B | 0 | NVCC\_SD2, 1V8, Input with PD | AD29 | SD2\_CD\_B |
| J6 | Pin37 | SD2\_DATA2 | USDHC2\_DATA2 | 0 | NVCC\_SD2, 1V8, Input with PD | AA26 | SD2\_DATA2 |
| J6 | Pin38 | SD2\_CLK | USDHC2\_CLK | 0 | NVCC\_SD2, 1V8, Input with PD | AB29 | SD2\_CLK |
| J6 | Pin40 | SD2\_CMD | USDHC2\_CMD | 0 | NVCC\_SD2, 1V8, Input with PD | AB28 | SD2\_CMD |
| J6 | Pin42 | SD2\_DATA3 | USDHC2\_DATA3 | 0 | NVCC\_SD2, 1V8, Input with PD | AA25 | SD2\_DATA3 |

**4.4.3 uSDHC3 signals**

uSDHC controller uSDHC3 is not exposed externally. uSDHC3 is used internally for the eMMC on the SOM. It’s not exposed.

**4.5 USB3.0**

The DEBIX SOM A consists of two USB controllers and PHYs that support USB3.0 and USB2.0

Each USB3.0 module includes the following features:

* Complies with USB specification rev 3.0 (xHCI compatible)
* Supports operation as a standalone USB host controller
* USB dual-role operation and can be configured as host or device
* Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations.
* Supports operation as a standalone single port USB
* Supports four programmable, bidirectional USB endpoints
* Supports system memory interface with 40-bit addressing capability

The USB 3.0 module operates in following modes.

* Host Mode: SS/HS/FS/LS
* Device Mode: SS/HS/FS

**4.5.1 USB Port1 interface signals**

USB Port1 is used as USB OTG by default

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **Notes** | **BALL** | **BALL\_NAME** |
| J3 | Pin8 | GPIO1\_IO13 | USB1\_OC | 1 | NVCC\_GPIO, 1V8, Input with PD | A6 | GPIO1\_IO13 |
| J3 | Pin10 | GPIO1\_IO12 | USB1\_PWR | 1 | NVCC\_GPIO, 1V8, Input with PD | A5 | GPIO1\_IO12 |
| J3 | Pin13 | USB1\_RXN | USB1\_RX\_N | 0 | VDD\_USB\_3P3, 3V3, Input | B9 | USB1\_RX\_N |
| J3 | Pin14 | GPIO1\_IO10 | USB1\_ID | 1 | NVCC\_GPIO, 1V8, Input with PD | B7 | GPIO1\_IO10 |
| J3 | Pin15 | USB1\_RXP | USB1\_RX\_P | 0 | VDD\_USB\_3P3, 3V3, Input | A9 | USB1\_RX\_P |
| J3 | Pin19 | USB1\_TXN | USB1\_TX\_N | 0 | VDD\_USB\_3P3, 3V3, Output | B10 | USB1\_TX\_N |
| J3 | Pin21 | USB1\_TXP | USB1\_TX\_P | 0 | VDD\_USB\_3P3, 3V3, Output | A10 | USB1\_TX\_P |
| J3 | Pin24 | USB1\_DN | USB1\_D\_N | 0 | VDD\_USB\_3P3, 3V3, Input | E10 | USB1\_D\_N |
| J3 | Pin26 | USB1\_DP | USB1\_D\_P | 0 | VDD\_USB\_3P3, 3V3, Input | D10 | USB1\_D\_P |
| J3 | Pin36 | USB1\_VBUS\_3V3 | USB1\_VBUS | 0 | VDD\_USB\_3P3, 3.3V,  Input | A11 | USB1\_VBUS |

**4.5.2 USB Port2 interface signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **Notes** | **BALL** | **BALL\_NAME** |
| J3 | Pin4 | GPIO1\_IO15 | USB2\_OC | 1 | NVCC\_GPIO, 1V8, Input with PD | B5 | GPIO1\_IO15 |
| J3 | Pin6 | GPIO1\_IO14 | USB2\_PWR | 1 | NVCC\_GPIO, 1V8, Input with PD | A4 | GPIO1\_IO14 |
| J3 | Pin12 | GPIO1\_IO11 | USB2\_ID | 1 | NVCC\_GPIO, 1V8, Input with PD | D8 | GPIO1\_IO11 |
| J3 | Pin25 | USB2\_RXN | USB2\_RX\_N | 0 | VDD\_USB\_3P3, 3V3, Input | B12 | USB2\_RX\_N |
| J3 | Pin27 | USB2\_RXP | USB2\_RX\_P | 0 | VDD\_USB\_3P3, 3V3, Input | A12 | USB2\_RX\_P |
| J3 | Pin30 | USB2\_DN | USB2\_D\_N | 0 | VDD\_USB\_3P3, 3V3, Input | E14 | USB2\_D\_N |
| J3 | Pin31 | USB2\_TXN | USB2\_TX\_N | 0 | VDD\_USB\_3P3, 3V3, Output | B13 | USB2\_TX\_N |
| J3 | Pin32 | USB2\_DP | USB2\_D\_P | 0 | VDD\_USB\_3P3, 3V3, Input | D14 | USB2\_D\_P |
| J3 | Pin33 | USB2\_TXP | USB2\_TX\_P | 0 | VDD\_USB\_3P3, 3V3, Output | A13 | USB2\_TX\_P |
| J3 | Pin38 | USB2\_VBUS\_3V3 | USB2\_VBUS | 0 | VDD\_USB\_3P3, 3.3V, Input | D12 | USB2\_VBUS |

**4.6 PCIe**

The DEBIX SOM A exposes one PCI Express Gen 3.0 single lane interface

The PCIe controller implementation is compatible with the following standards:

* PCI Express Base Specification, Revision 4.0, Version 0.7
* PCI Local Bus Specification, Revision 3.0
* PCI Bus Power Management Specification, Revision 1.2
* PCI Express Card Electromechanical Specification, Revision 1.1

The supported features in a Samsung PCIe PHY IP core are:

* PCI Express Base Specification 4.0 compliance
* 2.5Gb/s, 5.0Gb/s, and 8.0Gb/s Serializer/Deserializer
* PHY Interface for the PCI Express Architecture, Version 4.2 compliance
* Receiver Detection
* Spread Spectrum Clocking in Transmitter and Receiver
* Separate Refclk Independent SSC (SRIS) Architecture
* Continuous-Time Linear Equalizer and 5-tap adaptive Decision-Feedback Equalizer

**4.6.1 PCIE signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **Notes** | **BALL** | **BALL\_NAME** |
| J3 | Pin37 | PCIE\_CLKN | PCIE\_REF\_PAD\_CLK\_N | 0 | VDD\_PCI\_1P8, 1V8, High-Z | E16 | PCIE\_REF\_PAD\_CLK\_N |
| J3 | Pin39 | PCIE\_CLKP | PCIE\_REF\_PAD\_CLK\_P | 0 | VDD\_PCI\_1P8, 1V8, High-Z | D16 | PCIE\_REF\_PAD\_CLK\_P |
| J3 | Pin43 | PCIE\_RXN | PCIE\_RXN\_N | 0 | VDD\_PCI\_1P8, 1V8, Input, High-Z | B14 | PCIE\_RXN\_N |
| J3 | Pin45 | PCIE\_RXP | PCIE\_RXN\_P | 0 | VDD\_PCI\_1P8, 1V8, Input, High-Z | A14 | PCIE\_RXN\_P |
| J3 | Pin49 | PCIE\_TXN | PCIE\_TXN\_N | 0 | VDD\_PCI\_1P8, 1V8, Output, High-Z | B15 | PCIE\_TXN\_N |
| J3 | Pin51 | PCIE\_TXP | PCIE\_TXN\_P | 0 | VDD\_PCI\_1P8, 1V8, Output, High-Z | A15 | PCIE\_TXN\_P |

**4.6.2 PCIE Side Band Signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **Notes** | **BALL** | **BALL\_NAME** |
| J5 | Pin11 | I2C4\_SCL | PCIE\_CLKREQ\_B | 2 | NVCC\_I2C\_UART, 1V8, Input with PD | AF8 | I2C4\_SCL |
| J5 | Pin18 | UART4\_RXD | PCIE\_CLKREQ\_B | 2 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |

**4.7 audio**

DEBIX SOM A provides 6 external SAI(Synchronous audio interface) module, supporting I2S, AC97, TDM, codec/DSP and DSD interfaces. In addition to the general audio input/output functions, the audio interfaces support the following features:

* SAI1 supports to up to 8 I2S/TDM Tx lanes and 8 I2S/TDM Rx lanes at 768kHz/32-bit
* SAI2/5 supports to up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 768kHz/32-bit
* SAI3 supports up to 4-channels TX (2 lanes) and 4-channels RX (2 lanes) at 768kHz/32-bit
* SAI6 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at

768kHz/32-bit when multiplexed on SAI1, or up to 384kHz/32-bit when multiplexed on Ethernet primary pins

* SAI7 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384kHz/32-bit
* SPDIF supports raw capture mode that can save all incoming bits into an audio buffer
* PDM supports up to 8-channels (4 lanes)
* Hifi4 Audio DSP, operating up to 800 MHz

**4.7.2 Serial audio interface**

The Synchronous Audio Interface (SAI) provides an interface that supports full-duplex

serial interfaces with frame synchronization formats such as I2S, AC97, TDM, and codec/DSP interfaces.

The following table lists the signal definition of SAI interface signals

SAI interface signal definition:

|  |  |  |
| --- | --- | --- |
| **NAME** | **Function** | **DIR** |
| SAI\_TXC | Transmit Bit Clock.  The bit clock is an input when externally generated and an output when internally generated. | I/O |
| SAI\_TXFS | Transmit Frame Sync.  The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated | I/O |
| SAI\_TXD | Transmit Data.  The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word. | O |
| SAI\_RXC | Receive Bit Clock.  The bit clock is an input when externally generated and an output when internally generated | I/O |
| SAI\_RXFS | Receive Frame Sync.  The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated | I/O |
| SAI\_RXD | Receive Data.  The receive data is sampled synchronously by the bit clock | I |

**4.7.2.1 SAI1 signals**

Serial audio interface 1 signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin42 | SAI1\_MCLK | AUDIOMIX\_SAI1\_MCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE12 | SAI1\_MCLK |
| J5 | Pin24 | SAI1\_RXC | AUDIOMIX\_SAI1\_RX\_BCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH8 | SAI1\_RXC |
| J5 | Pin26 | SAI1\_RXD0 | AUDIOMIX\_SAI1\_RX\_DATA00 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC10 | SAI1\_RXD0 |
| J5 | Pin28 | SAI1\_RXD1 | AUDIOMIX\_SAI1\_RX\_DATA01 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF10 | SAI1\_RXD1 |
| J5 | Pin30 | SAI1\_RXD2 | AUDIOMIX\_SAI1\_RX\_DATA02 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH9 | SAI1\_RXD2 |
| J5 | Pin32 | SAI1\_RXD3 | AUDIOMIX\_SAI1\_RX\_DATA03 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ8 | SAI1\_RXD3 |
| J5 | Pin34 | SAI1\_RXD4 | AUDIOMIX\_SAI1\_RX\_DATA04 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD10 | SAI1\_RXD4 |
| J5 | Pin36 | SAI1\_RXD5 | AUDIOMIX\_SAI1\_RX\_DATA05 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J5 | Pin38 | SAI1\_RXD6 | AUDIOMIX\_SAI1\_RX\_DATA06 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH10 | SAI1\_RXD6 |
| J5 | Pin40 | SAI1\_RXD7 | AUDIOMIX\_SAI1\_RX\_DATA07 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |
| J5 | Pin22 | SAI1\_RXFS | AUDIOMIX\_SAI1\_RX\_SYNC | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ9 | SAI1\_RXFS |
| J5 | Pin36 | SAI1\_RXD5 | AUDIOMIX\_SAI1\_RX\_SYNC | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J5 | Pin17 | SAI1\_TXC | AUDIOMIX\_SAI1\_TX\_BCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ12 | SAI1\_TXC |
| J5 | Pin50 | SAI5\_MCLK | AUDIOMIX\_SAI1\_TX\_BCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin42 | SAI1\_MCLK | AUDIOMIX\_SAI1\_TX\_BCLK | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE12 | SAI1\_MCLK |
| J5 | Pin19 | SAI1\_TXD0 | AUDIOMIX\_SAI1\_TX\_DATA00 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ11 | SAI1\_TXD0 |
| J5 | Pin46 | SAI5\_RXFS | AUDIOMIX\_SAI1\_TX\_DATA00 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC14 | SAI5\_RXFS |
| J5 | Pin21 | SAI1\_TXD1 | AUDIOMIX\_SAI1\_TX\_DATA01 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ10 | SAI1\_TXD1 |
| J5 | Pin48 | SAI5\_RXC | AUDIOMIX\_SAI1\_TX\_DATA01 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J5 | Pin26 | SAI1\_RXD0 | AUDIOMIX\_SAI1\_TX\_DATA01 | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC10 | SAI1\_RXD0 |
| J5 | Pin23 | SAI1\_TXD2 | AUDIOMIX\_SAI1\_TX\_DATA02 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH11 | SAI1\_TXD2 |
| J5 | Pin39 | SAI5\_RXD0 | AUDIOMIX\_SAI1\_TX\_DATA02 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J5 | Pin25 | SAI1\_TXD3 | AUDIOMIX\_SAI1\_TX\_DATA03 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD12 | SAI1\_TXD3 |
| J5 | Pin41 | SAI5\_RXD1 | AUDIOMIX\_SAI1\_TX\_DATA03 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |
| J5 | Pin27 | SAI1\_TXD4 | AUDIOMIX\_SAI1\_TX\_DATA04 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH13 | SAI1\_TXD4 |
| J5 | Pin43 | SAI5\_RXD2 | AUDIOMIX\_SAI1\_TX\_DATA04 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin40 | SAI1\_RXD7 | AUDIOMIX\_SAI1\_TX\_DATA04 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |
| J5 | Pin29 | SAI1\_TXD5 | AUDIOMIX\_SAI1\_TX\_DATA05 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH14 | SAI1\_TXD5 |
| J5 | Pin45 | SAI5\_RXD3 | AUDIOMIX\_SAI1\_TX\_DATA05 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin31 | SAI1\_TXD6 | AUDIOMIX\_SAI1\_TX\_DATA06 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC12 | SAI1\_TXD6 |
| J5 | Pin33 | SAI1\_TXD7 | AUDIOMIX\_SAI1\_TX\_DATA07 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ13 | SAI1\_TXD7 |
| J5 | Pin35 | SAI1\_TXFS | UDIOMIX\_SAI1\_TX\_SYNC | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF12 | SAI1\_TXFS |
| J5 | Pin41 | SAI5\_RXD1 | AUDIOMIX\_SAI1\_TX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |
| J5 | Pin43 | SAI5\_RXD2 | AUDIOMIX\_SAI1\_TX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin45 | SAI5\_RXD3 | AUDIOMIX\_SAI1\_TX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin40 | SAI1\_RXD7 | AUDIOMIX\_SAI1\_TX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |

**4.7.2.2 SAI2 Signals**

Serial Audio Interface 2 signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin56 | SAI2\_MCLK | AUDIOMIX\_SAI2\_MCLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin54 | SAI2\_RXC | AUDIOMIX\_SAI2\_RX\_BCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin53 | SAI2\_RXD | AUDIOMIX\_SAI2\_RX\_DATA00 | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_SAI2\_RX\_DATA01 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin52 | SAI2\_RXFS | AUDIOMIX\_SAI2\_RX\_DATA01 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin60 | SAI3\_RXC | AUDIOMIX\_SAI2\_RX\_DATA02 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin64 | SAI3\_RXD | AUDIOMIX\_SAI2\_RX\_DATA03 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J5 | Pin52 | SAI2\_RXFS | AUDIOMIX\_SAI2\_RX\_SYNC | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin47 | SAI2\_TXC | AUDIOMIX\_SAI2\_TX\_BCLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH15 | SAI2\_TXC |
| J5 | Pin51 | SAI2\_TXD | AUDIOMIX\_SAI2\_TX\_DATA00 | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin57 | SAI3\_TXFS | AUDIOMIX\_SAI2\_TX\_DATA01 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J5 | Pin53 | SAI2\_RXD | AUDIOMIX\_SAI2\_TX\_DATA01 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin49 | SAI2\_TXFS | AUDIOMIX\_SAI2\_TX\_DATA01 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J5 | Pin55 | SAI3\_TXC | AUDIOMIX\_SAI2\_TX\_DATA02 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J5 | Pin59 | SAI3\_TXD | AUDIOMIX\_SAI2\_TX\_DATA03 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J5 | Pin49 | SAI2\_TXFS | AUDIOMIX\_SAI2\_TX\_SYNC | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |

**4.7.2.3 SAI3 signals**

Serial Audio interface 3 signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin58 | SAI3\_MCLK | AUDIOMIX\_SAI3\_MCLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |
| J4 | Pin34 | NAND\_DQS | AUDIOMIX\_SAI3\_MCLK | 2 | NVCC\_NAND, 1V8, Input with PD | R26 | NAND\_DQS |
| J5 | Pin56 | SAI2\_MCLK | AUDIOMIX\_SAI3\_MCLK | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin60 | SAI3\_RXC | AUDIOMIX\_SAI3\_RX\_BCLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin64 | SAI3\_RXD | AUDIOMIX\_SAI3\_RX\_DATA00 | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J6 | Pin46 | QSPIA\_DATA0 | AUDIOMIX\_SAI3\_RX\_DATA00 | 2 | NVCC\_NAND, 1V8, Input with PD | R25 | NAND\_DATA00 |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_SAI3\_RX\_DATA01 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_SAI3\_RX\_SYNC | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin55 | SAI3\_TXC | AUDIOMIX\_SAI3\_TX\_BCLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J6 | Pin41 | QSPIA\_SCLK | AUDIOMIX\_SAI3\_TX\_BCLK | 2 | NVCC\_NAND, 1V8, Input with PD | N25 | NAND\_ALE |
| J5 | Pin59 | SAI3\_TXD | AUDIOMIX\_SAI3\_TX\_DATA00 | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J6 | Pin44 | QSPIA\_nSS0 | AUDIOMIX\_SAI3\_TX\_DATA00 | 2 | NVCC\_NAND, 1V8, Input with PD | L26 | NAND\_CE0\_B |
| J5 | Pin57 | SAI3\_TXFS | AUDIOMIX\_SAI3\_TX\_DATA01 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J5 | Pin57 | SAI3\_TXFS | AUDIOMIX\_SAI3\_TX\_SYNC | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J6 | Pin48 | QSPIA\_DATA1 | AUDIOMIX\_SAI3\_TX\_SYNC | 2 | NVCC\_NAND, 1V8, Input with PD | L25 | NAND\_DATA01 |

**4.7.2.4 SAI5 signals**

Serial Audio Interface 5 signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin50 | SAI5\_MCLK | AUDIOMIX\_SAI5\_MCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin56 | SAI2\_MCLK | AUDIOMIX\_SAI5\_MCLK | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin58 | SAI3\_MCLK | AUDIOMIX\_SAI5\_MCLK | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |
| J5 | Pin48 | SAI5\_RXC | AUDIOMIX\_SAI5\_RX\_BCLK | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J5 | Pin60 | SAI3\_RXC | AUDIOMIX\_SAI5\_RX\_BCLK | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin39 | SAI5\_RXD0 | AUDIOMIX\_SAI5\_RX\_DATA00 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J5 | Pin64 | SAI3\_RXD | AUDIOMIX\_SAI5\_RX\_DATA00 | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J5 | Pin41 | SAI5\_RXD1 | AUDIOMIX\_SAI5\_RX\_DATA01 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |
| J5 | Pin57 | SAI3\_TXFS | AUDIOMIX\_SAI5\_RX\_DATA01 | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J5 | Pin43 | SAI5\_RXD2 | AUDIOMIX\_SAI5\_RX\_DATA02 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin55 | SAI3\_TXC | AUDIOMIX\_SAI5\_RX\_DATA02 | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J5 | Pin45 | SAI5\_RXD3 | AUDIOMIX\_SAI5\_RX\_DATA03 | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin59 | SAI3\_TXD | AUDIOMIX\_SAI5\_RX\_DATA03 | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J5 | Pin46 | SAI5\_RXFS | AUDIOMIX\_SAI5\_RX\_SYNC | 0 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC14 | SAI5\_RXFS |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_SAI5\_RX\_SYNC | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin54 | SAI2\_RXC | AUDIOMIX\_SAI5\_TX\_BCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin43 | SAI5\_RXD2 | AUDIOMIX\_SAI5\_TX\_BCLK | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin53 | SAI2\_RXD | AUDIOMIX\_SAI5\_TX\_DATA00 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin45 | SAI5\_RXD3 | AUDIOMIX\_SAI5\_TX\_DATA00 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin49 | SAI2\_TXFS | AUDIOMIX\_SAI5\_TX\_DATA01 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J5 | Pin52 | SAI2\_RXFS | AUDIOMIX\_SAI5\_TX\_DATA01 | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin47 | SAI2\_TXC | AUDIOMIX\_SAI5\_TX\_DATA02 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH15 | SAI2\_TXC |
| J5 | Pin51 | SAI2\_TXD | AUDIOMIX\_SAI5\_TX\_DATA03 | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin52 | SAI2\_RXFS | AUDIOMIX\_SAI5\_TX\_SYNC | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin41 | SAI5\_RXD1 | AUDIOMIX\_SAI5\_TX\_SYNC | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |

**4.7.2.5 SAI6 signals**

Serial Audio Interface 6 signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin40 | SAI1\_RXD7 | AUDIOMIX\_SAI6\_MCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |
| J5 | Pin33 | SAI1\_TXD7 | AUDIOMIX\_SAI6\_MCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ13 | SAI1\_TXD7 |
| J6 | Pin8 | ENET\_TX\_CTL | AUDIOMIX\_SAI6\_MCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AF24 | ENET\_TX\_CTL |
| J5 | Pin27 | SAI1\_TXD4 | AUDIOMIX\_SAI6\_RX\_BCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH13 | SAI1\_TXD4 |
| J6 | Pin12 | ENET\_TD0 | AUDIOMIX\_SAI6\_RX\_BCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AC25 | ENET\_TD0 |
| J5 | Pin34 | SAI1\_RXD4 | AUDIOMIX\_SAI6\_RX\_BCLK | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD10 | SAI1\_RXD4 |
| J5 | Pin29 | SAI1\_TXD5 | AUDIOMIX\_SAI6\_RX\_DATA00 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH14 | SAI1\_TXD5 |
| J6 | Pin16 | ENET\_TD2 | AUDIOMIX\_SAI6\_RX\_DATA00 | 2 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J5 | Pin36 | SAI1\_RXD5 | AUDIOMIX\_SAI6\_RX\_DATA00 | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J5 | Pin31 | SAI1\_TXD6 | AUDIOMIX\_SAI6\_RX\_SYNC | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC12 | SAI1\_TXD6 |
| J6 | Pin14 | ENET\_TD1 | AUDIOMIX\_SAI6\_RX\_SYNC | 2 | NVCC\_ENET, 1V8, Input with PD | AE26 | ENET\_TD1 |
| J5 | Pin38 | SAI1\_RXD6 | AUDIOMIX\_SAI6\_RX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH10 | SAI1\_RXD6 |
| J5 | Pin34 | SAI1\_RXD4 | AUDIOMIX\_SAI6\_TX\_BCLK | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD10 | SAI1\_RXD4 |
| J6 | Pin18 | ENET\_TD3 | AUDIOMIX\_SAI6\_TX\_BCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AD24 | ENET\_TD3 |
| J5 | Pin27 | SAI1\_TXD4 | AUDIOMIX\_SAI6\_TX\_BCLK | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH13 | SAI1\_TXD4 |
| J5 | Pin36 | SAI1\_RXD5 | AUDIOMIX\_SAI6\_TX\_DATA00 | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J6 | Pin4 | ENET\_MDC | AUDIOMIX\_SAI6\_TX\_DATA00 | 2 | NVCC\_ENET, 1V8, Input with PD | AH28 | ENET\_MDC |
| J5 | Pin29 | SAI1\_TXD5 | AUDIOMIX\_SAI6\_TX\_DATA00 | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH14 | SAI1\_TXD5 |
| J5 | Pin38 | SAI1\_RXD6 | AUDIOMIX\_SAI6\_TX\_SYNC | 1 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH10 | SAI1\_RXD6 |
| J6 | Pin6 | ENET\_MDIO | AUDIOMIX\_SAI6\_TX\_SYNC | 2 | NVCC\_ENET, 1V8, Input with PD | AH29 | ENET\_MDIO |
| J5 | Pin31 | SAI1\_TXD6 | AUDIOMIX\_SAI6\_TX\_SYNC | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC12 | SAI1\_TXD6 |

**4.7.2.6 SAI7 signals**

Serial Audio Interface 7 signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J6 | Pin30 | ENET\_RD3 | AUDIOMIX\_SAI7\_MCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AF28 | ENET\_RD3 |
| J5 | Pin69 | ECSPI2\_MISO | AUDIOMIX\_SAI7\_MCLK | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J6 | Pin28 | ENET\_RD2 | AUDIOMIX\_SAI7\_RX\_BCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AF29 | ENET\_RD2 |
| J5 | Pin76 | UART3\_TXD | AUDIOMIX\_SAI7\_RX\_BCLK | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC20 | ECSPI1\_MOSI |
| J6 | Pin24 | ENET\_RD0 | AUDIOMIX\_SAI7\_RX\_DATA00 | 2 | NVCC\_ENET, 1V8, Input with PD | AG29 | ENET\_RD0 |
| J5 | Pin72 | UART3\_CTS | AUDIOMIX\_SAI7\_RX\_DATA00 | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD20 | ECSPI1\_MISO |
| J6 | Pin26 | ENET\_RD1 | AUDIOMIX\_SAI7\_RX\_SYNC | 2 | NVCC\_ENET, 1V8, Input with PD | AG28 | ENET\_RD1 |
| J5 | Pin78 | UART3\_RXD | AUDIOMIX\_SAI7\_RX\_SYNC | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF20 |  |
| J6 | Pin22 | ENET\_RXC | AUDIOMIX\_SAI7\_TX\_BCLK | 2 | NVCC\_ENET, 1V8, Input with PD | AE29 | ENET\_RXC |
| J5 | Pin63 | ECSPI2\_SCLK | AUDIOMIX\_SAI7\_TX\_BCLK | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH21 | ECSPI2\_SCLK |
| J6 | Pin10 | ENET\_TXC | AUDIOMIX\_SAI7\_TX\_DATA00 | 2 | NVCC\_ENET, 1V8, Input with PD | AE24 | ENET\_TXC |
| J5 | Pin67 | ECSPI2\_MOSI | AUDIOMIX\_SAI7\_TX\_DATA00 | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ21 | ECSPI2\_MOSI |
| J6 | Pin20 | ENET\_RX\_CTL | AUDIOMIX\_SAI7\_TX\_SYNC | 2 | NVCC\_ENET, 1V8, Input with PD | AE28 | ENET\_RX\_CTL |
| J5 | Pin74 | UART3\_RTS | AUDIOMIX\_SAI7\_TX\_SYNC | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE20 | ECSPI1\_SS0 |

**4.7.3 PDM-Microphone Interface(MICFIL)**

The Pulse Density Modulated Microphone Interface (MICFIL) is a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.

The PDM Microphone Interface consists of the following:

* an input interface for each pair of PDM microphones.
* a decimation filter by channel
* a FIFO by channel
* a time generation unit
* shared interfaces to DMA, interrupts and SoC
* A Hardware Voice Activity Detector (HWVAD)

The PDM Microphone Interface (MICFIL) includes the following features:

* Decimation filters:
* Fixed-point filtering
* 24-bit PCM audio output
* Internal clock divider for a programmable PDM clock generation
* Full or partial set of channels operation with individual enable control
* Programmable decimation rate
* Programmable DC remover
* Range adjustement capability
* FIFOs with interrupt and DMA capability
* Each FIFO with 32 entries length
* Hardware Voice Activity Detector (HWVAD)
* Interrupt capability
* Zero-Crossing Detection (ZCD) option

PDM interface signals

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J6 | Pin14 | ENET\_TD1 | AUDIOMIX\_PDM\_BIT\_STREAM00 | 3 | NVCC\_ENET, 1V8, Input with PD | AE26 | ENET\_TD1 |
| J6 | Pin26 | ENET\_RD1 | AUDIOMIX\_PDM\_BIT\_STREAM00 | 3 | NVCC\_ENET, 1V8, Input with PD | AG28 | ENET\_RD1 |
| J5 | Pin26 | SAI1\_RXD0 | AUDIOMIX\_PDM\_BIT\_STREAM00 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC10 | SAI1\_RXD0 |
| J6 | Pin33 | SD2\_DATA0 | AUDIOMIX\_PDM\_BIT\_STREAM00 | 4 | NVCC\_SD2, 1V8, Input with PD | AC28 | SD2\_DATA0 |
| J5 | Pin39 | SAI5\_RXD0 | AUDIOMIX\_PDM\_BIT\_STREAM00 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_PDM\_BIT\_STREAM00 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J6 | Pin16 | ENET\_TD2 | AUDIOMIX\_PDM\_BIT\_STREAM01 | 3 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J6 | Pin24 | ENET\_RD0 | AUDIOMIX\_PDM\_BIT\_STREAM01 | 3 | NVCC\_ENET, 1V8, Input with PD | AG29 | ENET\_RD0 |
| J5 | Pin28 | SAI1\_RXD1 | AUDIOMIX\_PDM\_BIT\_STREAM01 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF10 | SAI1\_RXD1 |
| J6 | Pin35 | SD2\_DATA1 | AUDIOMIX\_PDM\_BIT\_STREAM01 | 4 | NVCC\_SD2, 1V8, Input with PD | AC29 | SD2\_DATA1 |
| J5 | Pin41 | SAI5\_RXD1 | AUDIOMIX\_PDM\_BIT\_STREAM01 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |
| J5 | Pin54 | SAI2\_RXC | AUDIOMIX\_PDM\_BIT\_STREAM01 | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin47 | SAI2\_TXC | AUDIOMIX\_PDM\_BIT\_STREAM01 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH15 | SAI2\_TXC |
| J5 | Pin64 | SAI3\_RXD | AUDIOMIX\_PDM\_BIT\_STREAM01 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J6 | Pin18 | ENET\_TD3 | AUDIOMIX\_PDM\_BIT\_STREAM02 | 3 | NVCC\_ENET, 1V8, Input with PD | AD24 | ENET\_TD3 |
| J6 | Pin22 | ENET\_RXC | AUDIOMIX\_PDM\_BIT\_STREAM02 | 3 | NVCC\_ENET, 1V8, Input with PD | AE29 | ENET\_RXC |
| J5 | Pin30 | SAI1\_RXD2 | AUDIOMIX\_PDM\_BIT\_STREAM02 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH9 | SAI1\_RXD2 |
| J6 | Pin37 | SD2\_DATA2 | AUDIOMIX\_PDM\_BIT\_STREAM02 | 4 | NVCC\_SD2, 1V8, Input with PD | AA26 | SD2\_DATA2 |
| J5 | Pin43 | SAI5\_RXD2 | AUDIOMIX\_PDM\_BIT\_STREAM02 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin52 | SAI2\_RXFS | AUDIOMIX\_PDM\_BIT\_STREAM02 | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin49 | SAI2\_TXFS | AUDIOMIX\_PDM\_BIT\_STREAM02 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J5 | Pin55 | SAI3\_TXC | AUDIOMIX\_PDM\_BIT\_STREAM02 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J6 | Pin6 | ENET\_MDIO | AUDIOMIX\_PDM\_BIT\_STREAM03 | 3 | NVCC\_ENET, 1V8, Input with PD | AH29 | ENET\_MDIO |
| J6 | Pin20 | ENET\_RX\_CTL | AUDIOMIX\_PDM\_BIT\_STREAM03 | 3 | NVCC\_ENET, 1V8, Input with PD | AE28 | ENET\_RX\_CTL |
| J5 | Pin32 | SAI1\_RXD3 | AUDIOMIX\_PDM\_BIT\_STREAM03 | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ8 | SAI1\_RXD3 |
| J6 | Pin42 | SD2\_DATA3 | AUDIOMIX\_PDM\_BIT\_STREAM3 | 4 | NVCC\_SD2, 1V8, Input with PD | AA25 | SD2\_DATA3 |
| J5 | Pin45 | SAI5\_RXD3 | AUDIOMIX\_PDM\_BIT\_STREAM03 | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin53 | SAI2\_RXD | AUDIOMIX\_PDM\_BIT\_STREAM03 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin57 | SAI3\_TXFS | AUDIOMIX\_PDM\_BIT\_STREAM03 | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J6 | Pin12 | ENET\_TD0 | AUDIOMIX\_PDM\_CLK | 3 | NVCC\_ENET, 1V8, Input with PD | AC25 | ENET\_TD0 |
| J6 | Pin28 | ENET\_RD2 | AUDIOMIX\_PDM\_CLK | 3 | NVCC\_ENET, 1V8, Input with PD | AF29 | ENET\_RD2 |
| J5 | Pin24 | SAI1\_RXC | AUDIOMIX\_PDM\_CLK | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH8 | SAI1\_RXC |
| J5 | Pin33 | SAI1\_TXD7 | AUDIOMIX\_PDM\_CLK | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ13 | SAI1\_TXD7 |
| J6 | Pin40 | SD2\_CMD | AUDIOMIX\_PDM\_CLK | 4 | NVCC\_SD2, 1V8, Input with PD | AB28 | SD2\_CMD |
| J5 | Pin48 | SAI5\_RXC | AUDIOMIX\_PDM\_CLK | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J5 | Pin60 | SAI3\_RXC | AUDIOMIX\_PDM\_CLK | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |

**4.7.4 SPDIF- Sony Philips Digital Interface Format**

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.

The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.

For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

SPDIF interface signals:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin70 | SPDIF\_EXT\_CLK | AUDIOMIX\_SPDIF1\_EXT\_CLK | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC18 | SPDIF\_EXT\_CLK |
| J5 | Pin59 | SAI3\_TXD | AUDIOMIX\_SPDIF1\_EXT\_CLK | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J5 | Pin68 | SPDIF\_RX | AUDIOMIX\_SPDIF1\_IN | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J6 | Pin30 | ENET\_RD3 | AUDIOMIX\_SPDIF1\_IN | 3 | NVCC\_ENET, 1V8, Input with PD | AF28 | ENET\_RD3 |
| J6 | Pin42 | SD2\_DATA3 | AUDIOMIX\_SPDIF1\_IN | 3 | NVCC\_SD2, 1V8, Input with PD | AA25 | SD2\_DATA3 |
| J5 | Pin62 | SAI3\_RXFS | AUDIOMIX\_SPDIF1\_IN | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin58 | SAI3\_MCLK | AUDIOMIX\_SPDIF1\_IN | 6 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |
| J5 | Pin66 | SPDIF\_TX | AUDIOMIX\_SPDIF1\_OUT | 0 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J6 | Pin8 | ENET\_TX\_CTL | AUDIOMIX\_SPDIF1\_OUT | 3 | NVCC\_ENET, 1V8, Input with PD | AF24 | ENET\_TX\_CTL |
| J6 | Pin37 | SD2\_DATA2 | AUDIOMIX\_SPDIF1\_OUT | 3 | NVCC\_SD2, 1V8, Input with PD | AA26 | SD2\_DATA2 |
| J5 | Pin58 | SAI3\_MCLK | AUDIOMIX\_SPDIF1\_OUT | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |

**4.8 UART**

DEBIX SOM A provides up to 4 UART interfaces, some of which are multiplexed with other peripherals.

The UART includes the following features:

* High-speed TIA/EIA-232-F compatible, up to Mbit/s
* Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
* 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
* 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
* 1 or 2 stop bits
* Programmable parity (even, odd, and no parity)
* Hardware flow control support for request to send (RTS\_B) and clear to send (CTS\_B) signals
* RS-485 driver direction control via CTS\_B signal
* Edge-selectable RTS\_B and edge-detect interrupts
* Status flags for various flow control and FIFO states
* Voting logic for improved noise immunity (16x oversampling)
* Transmitter FIFO empty interrupt suppression
* UART internal clocks enable/disable
* Auto baud rate detection (up to 115.2 Kbit/s)
* Receiver and transmitter enable/disable for power saving
* RX\_DATA input and TX\_DATA output can be inverted respectively in RS-232/RS-485 mode
* DCE/DTE capability
* RTS\_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
* Maskable interrupts
* Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
* Escape character sequence detection
* Software reset (SRST\_B)
* Two independent, 32-entry FIFOs for transmit and receive
* The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

UART I/O configuration mode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Port** | **DTE mode** | | **DCE mode** | |
| **Direction** | **Description** | **Direction** | **Description** |
| UARTx\_RTS\_B | Output | UARTx\_RTS\_B from DTE to DCE | Input | UARTx\_RTS\_B from DTE to DCE |
| UARTx\_CTS\_B | Input | UARTx\_CTS\_B from DCE to DTE | Output | UARTx\_CTS from DCE to DTE |
| UARTx\_TX\_DATA | Input | Serial data from DCE to DTE | Output | Serial data from DCE to DTE |
| UARTx\_RX\_DATA | Output | Serial data from DCE to DTE | Output | Serial data from DCE to DTE |

**4.8.1 UART1 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin8 | UART1\_CTS | UART1\_CTS\_B | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AE6 | UART3\_RXD |
| J4 | Pin73 | SD1\_DATA1 | UART1\_CTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | Y28 | SD1\_DATA1 |
| J5 | Pin49 | SAI2\_TXFS | UART1\_CTS\_B | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J5 | Pin10 | UART1\_RTS | UART1\_RTS\_B | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ4 | UART3\_TXD |
| J4 | Pin71 | SD1\_DATA0 | UART1\_RTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | Y29 | SD1\_DATA0 |
| J5 | Pin53 | SAI2\_RXD | UART1\_RTS\_B | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin6 | UART1\_RXD | UART1\_RX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AD6 | UART1\_RXD |
| J4 | Pin69 | SD1\_CMD | UART1\_RX | 4 | NVCC\_SD1, 1V8, Input with PD | W29 | SD1\_CMD |
| J5 | Pin54 | SAI2\_RXC | UART1\_RX | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin4 | UART1\_TXD | UART1\_TX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ3 | UART1\_TXD |
| J4 | Pin67 | SD1\_CLK | UART1\_TX | 4 | NVCC\_SD1, 1V8, Input with PD | W28 | SD1\_CLK |
| J5 | Pin52 | SAI2\_RXFS | UART1\_TX | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |

**4.8.2 UART2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin18 | UART4\_RXD | UART2\_CTS\_B | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |
| J4 | Pin74 | SD1\_DATA5 | UART2\_CTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | AA29 | SD1\_DATA5 |
| J5 | Pin60 | SAI3\_RXC | UART2\_CTS\_B | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin16 | UART4\_TXD | UART2\_RTS\_B | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AH5 | UART4\_TXD |
| J4 | Pin72 | SD1\_DATA4 | UART2\_RTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | U26 | SD1\_DATA4 |
| J5 | Pin64 | SAI3\_RXD | UART2\_RTS\_B | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J5 | Pin14 | UART2\_RXD | UART2\_RX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AF6 | UART2\_RXD |
| J6 | Pin33 | SD2\_DATA0 | UART2\_RX | 3 | NVCC\_SD2, 1V8, Input with PD | AC28 | SD2\_DATA0 |
| J4 | Pin77 | SD1\_DATA3 | UART2\_RX | 4 | NVCC\_SD1, 1V8, Input with PD | V28 | SD1\_DATA3 |
| J5 | Pin57 | SAI3\_TXFS | UART2\_RX | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J5 | Pin12 | UART2\_TXD | UART2\_TX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AH4 | UART2\_TXD |
| J6 | Pin35 | SD2\_DATA1 | UART2\_TX | 3 | NVCC\_SD2, 1V8, Input with PD | AC29 | SD2\_DATA1 |
| J4 | Pin75 | SD1\_DATA2 | UART2\_TX | 4 | NVCC\_SD1, 1V8, Input with PD | V29 | SD1\_DATA2 |
| J5 | Pin55 | SAI3\_TXC | UART2\_TX | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |

**4.8.3 UART3 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin72 | UART3\_CTS | UART3\_CTS\_B | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD20 | ECSPI1\_MISO |
| J4 | Pin63 | SD1\_STROBE | UART3\_CTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | W26 | SD1\_STROBE |
| J5 | Pin74 | UART3\_RTS | UART3\_RTS\_B | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE20 | ECSPI1\_SS0 |
| J4 | Pin65 | SD1\_RESET\_B | UART3\_RTS\_B | 4 | NVCC\_SD1, 1V8, Input with PD | W25 | SD1\_RESET\_B |
| J5 | Pin8 | UART1\_CTS | UART3\_RX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AE6 | UART3\_RXD |
| J5 | Pin78 | UART3\_RXD | UART3\_RX | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF20 | ECSPI1\_SCLK |
| J4 | Pin78 | SD1\_DATA7 | UART3\_RX | 4 | NVCC\_SD1, 1V8, Input with PD | U25 | SD1\_DATA7 |
| J6 | Pin41 | QSPIA\_SCLK | UART3\_RX | 4 | NVCC\_NAND, 1V8, Input with PD | N25 | NAND\_ALE |
| J5 | Pin10 | UART1\_RTS | UART3\_TX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ4 | UART3\_TXD |
| J5 | Pin76 | UART3\_TXD | UART3\_TX | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC20 | ECSPI1\_MOSI |
| J4 | Pin76 | SD1\_DATA6 | UART3\_TX | 4 | NVCC\_SD1, 1V8, Input with PD | AA28 | SD1\_DATA6 |
| J6 | Pin44 | QSPIA\_nSS0 | UART3\_TX | 4 | NVCC\_NAND, 1V8, Input with PD | L26 | NAND\_CE0\_B |

**4.8.4 UART4 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin69 | ECSPI2\_MISO | UART4\_CTS\_B | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J6 | Pin50 | QSPIA\_DATA2 | UART4\_CTS\_B | 3 | NVCC\_NAND, 1V8, Input with PD | L24 | NAND\_DATA02 |
| J5 | Pin65 | ECSPI2\_SS0 | UART4\_RTS\_B | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ22 | ECSPI2\_SS0 |
| J6 | Pin52 | QSPIA\_DATA3 | UART4\_RTS\_B | 3 | NVCC\_NAND, 1V8, Input with PD | N24 | NAND\_DATA03 |
| J5 | Pin18 | UART4\_RXD | UART4\_RX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |
| J5 | Pin63 | ECSPI2\_SCLK | UART4\_RX | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH21 | ECSPI2\_SCLK |
| J6 | Pin38 | SD2\_CLK | UART4\_RX | 3 | NVCC\_SD2, 1V8, Input with PD | AB29 | SD2\_CLK |
| J6 | Pin46 | QSPIA\_DATA0 | UART4\_RX | 4 | NVCC\_NAND, 1V8, Input with PD | R25 | NAND\_DATA00 |
| J5 | Pin16 | UART4\_TXD | UART4\_TX | 0 | NVCC\_I2C\_UART, 1V8, Input with PD | AH5 | UART4\_TXD |
| J5 | Pin67 | ECSPI2\_MOSI | UART4\_TX | 1 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ21 | ECSPI2\_MOSI |
| J6 | Pin40 | SD2\_CMD | UART4\_TX | 3 | NVCC\_SD2, 1V8, Input with PD | AB28 | SD2\_CMD |
| J6 | Pin48 | QSPIA\_DATA1 | UART4\_TX | 4 | NVCC\_NAND, 1V8, Input with PD | L25 | NAND\_DATA01 |

**4.9 Flexible Controller Area Network**

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

The CAN protocol was primarily designed to be used as a vehicle serial data bus, meeting the specific real-time processing and reliable operation requirements in the EMI environment of a vehicle. The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads.

Signal description:

|  |  |  |
| --- | --- | --- |
| **Signal** | **Description** | **I/O** |
| CAN Rx | CAN receive pin | input |
| CAN Tx | CAN transmit pin | output |

* CAN Rx: This pin is the receive pin from the CAN bus transceiver. Dominant state is represented by logic level 0. Recessive state is represented by logic level 1.
* CAN Tx: This pin is the transmit pin to the CAN bus transceiver. Dominant state is represented by logic level 0. Recessive state is represented by logic level 1.

**4.9.1 FLEXCAN1 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin47 | SAI2\_TXC | CAN1\_RX | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH15 | SAI2\_TXC |
| J5 | Pin68 | SPDIF\_RX | CAN1\_RX | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J5 | Pin73 | HDMI\_DDC\_SDA | CAN1\_RX | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF22 | HDMI\_DDC\_SDA |
| J5 | Pin43 | SAI5\_RXD2 | CAN1\_RX | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin54 | SAI2\_RXC | CAN1\_TX | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin66 | SPDIF\_TX | CAN1\_TX | 4 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J5 | Pin71 | HDMI\_DDC\_SCL | CAN1\_TX | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC22 | HDMI\_DDC\_SCL |
| J5 | Pin41 | SAI5\_RXD1 | CAN1\_TX | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |

**4.9.2 FLEXCAN2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin56 | SAI2\_MCLK | CAN2\_RX | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin10 | UART1\_RTS | CAN2\_RX | 4 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ4 | UART3\_TXD |
| J5 | Pin75 | HDMI\_HPD | CAN2\_RX | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE22 | HDMI\_HPD |
| J5 | Pin50 | SAI5\_MCLK | CAN2\_RX | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin51 | SAI2\_TXD | CAN2\_TX | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin8 | UART1\_CTS | CAN2\_TX | 4 | NVCC\_I2C\_UART, 1V8, Input with PD | AE6 | UART3\_RXD |
| J5 | Pin77 | HDMI\_CEC | CAN2\_TX | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD22 | HDMI\_CEC |
| J5 | Pin45 | SAI5\_RXD3 | CAN2\_TX | 6 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |

**4.10 ECSPI - Enhanced Configurable SPI**

DEBIX SOM A exposes all ECSPI interfaces.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex,synchronous, four-wire serial communication block.

Key features of the ECSPI include:

* Full-duplex synchronous serial interface
* Master/Slave configurable
* One Chip Select (SS) signal
* Transfer continuation function allows unlimited length data transfers
* 32-bit wide by 64-entry FIFO for both transmit and receive data
* Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
* Direct Memory Access (DMA) support
* Refer to the product data sheet for the maximum operating frequency

**4.10.1 ECSPI1 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin72 | UART3\_CTS | ECSPI1\_MISO | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD20 | ECSPI1\_MISO |
| J5 | Pin3 | I2C2\_SCL | ECSPI1\_MISO | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AH6 | I2C2\_SCL |
| J5 | Pin76 | UART3\_TXD | ECSPI1\_MOSI | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC20 | ECSPI1\_MOSI |
| J5 | Pin78 | UART3\_RXD | ECSPI1\_SCLK | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF20 | ECSPI1\_SCLK |
| J5 | Pin74 | UART3\_RTS | ECSPI1\_SS0 | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE20 | ECSPI1\_SS0 |
| J5 | Pin5 | I2C2\_SDA | ECSPI1\_SS0 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AE8 | I2C2\_SDA |

**4.10.2 ECSPI2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin69 | ECSPI2\_MISO | ECSPI2\_MISO | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J6 | Pin42 | SD2\_DATA3 | ECSPI2\_MISO | 2 | NVCC\_SD2, 1V8, Input with PD | AA25 | SD2\_DATA3 |
| J5 | Pin11 | I2C4\_SCL | ECSPI2\_MISO | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AF8 | I2C4\_SCL |
| J5 | Pin67 | ECSPI2\_MOSI | ECSPI2\_MOSI | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ21 | ECSPI2\_MOSI |
| J6 | Pin40 | SD2\_CMD | ECSPI2\_MOSI | 2 | NVCC\_SD2, 1V8, Input with PD | AB28 | SD2\_CMD |
| J5 | Pin9 | I2C3\_SDA | ECSPI2\_MOSI | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ6 | I2C3\_SDA |
| J5 | Pin63 | ECSPI2\_SCLK | ECSPI2\_SCLK | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH21 | ECSPI2\_SCLK |
| J6 | Pin38 | SD2\_CLK | ECSPI2\_SCLK | 2 | NVCC\_SD2, 1V8, Input with PD | AB29 | SD2\_CLK |
| J5 | Pin7 | I2C3\_SCL | ECSPI2\_SCLK | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ7 | I2C3\_SCL |
| J5 | Pin65 | ECSPI2\_SS0 | ECSPI2\_SS0 | 0 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ22 | ECSPI2\_SS0 |
| J6 | Pin37 | SD2\_DATA2 | ECSPI2\_SS0 | 2 | NVCC\_SD2, 1V8, Input with PD | AA26 | SD2\_DATA2 |
| J5 | Pin13 | I2C4\_SDA | ECSPI2\_SS0 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AD8 | I2C4\_SDA |

**4.10.3 ECSPI3 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin14 | UART2\_RXD | ECSPI3\_MISO | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AF6 | UART2\_RXD |
| J5 | Pin4 | UART1\_TXD | ECSPI3\_MOSI | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ3 | UART1\_TXD |
| J5 | Pin6 | UART1\_RXD | ECSPI3\_SCLK | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AD6 | UART1\_RXD |
| J5 | Pin12 | UART2\_TXD | ECSPI3\_SS0 | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AH4 | UART2\_TXD |

**4.11 QSPI/FlexSPI - Quad Serial Peripheral Interface**

FlexSPI block supports following features:

* Flexible sequence engine (LUT table) to support various vendor devices
* Serial NOR Flash or other device with similar SPI protocol as Serial NOR Flash
* Serial NAND Flash
* HyperBus device (HyperFlash/HyperRAM)
* FPGA device
* Flash access mode
* Single/Dual/Quad/Octal mode
* SDR/DDR mode
* Individual/Parallel mode
* Support sampling clock mode:
* Internal dummy read strobe loopbacked internally
* Internal dummy read strobe loopbacked from pad
* Flash provided read strobe
* Automatic Data Learning to select correct sample clock phase
* Memory mapped read/write access by AHB Bus
* AHB RX Buffer implemented to reduce read latency. Total AHB RX Buffer size: 2048 KBytes
* 16 AHB masters supported with priority for read access
* 8 flexible and configurable buffers in AHB RX Buffer
* AHB TX Buffer implemented to buffer all write data from one AHB burst. AHB TX Buffer size: 64 Bytes
* All AHB masters share this AHB TX Buffer. No AHB master number limitation for Write Access.
* Software triggered Flash read/write access by IP Bus
* IP RX FIFO implemented to buffer all read data from External device. FIFO size: 512 Bytes
* IP TX FIFO implemented to buffer all Write data to External device. FIFO size: 1024 Bytes
* DMA support to fill IP TX FIFO
* DMA support to read IP RX FIFO
* SCLK stopped when reading flash data and IP RX FIFO is full
* SCLK stopped when writing flash data and IP TX FIFO is empty

**4.11.1 QSPIA signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J6 | Pin46 | QSPIA\_DATA0 | FLEXSPI\_A\_DATA00 | 1 | NVCC\_NAND, 1V8, Input with PD | R25 | NAND\_DATA00 |
| J6 | Pin48 | QSPIA\_DATA1 | FLEXSPI\_A\_DATA01 | 1 | NVCC\_NAND, 1V8, Input with PD | L25 | NAND\_DATA01 |
| J6 | Pin50 | QSPIA\_DATA2 | FLEXSPI\_A\_DATA02 | 1 | NVCC\_NAND, 1V8, Input with PD | L24 | NAND\_DATA02 |
| J6 | Pin52 | QSPIA\_DATA3 | FLEXSPI\_A\_DATA03 | 1 | NVCC\_NAND, 1V8, Input with PD | N24 | NAND\_DATA03 |
| J4 | Pin34 | NAND\_DQS | FLEXSPI\_A\_DQS | 1 | NVCC\_NAND, 1V8, Input with PD | R26 | NAND\_DQS |
| J6 | Pin41 | QSPIA\_SCLK | FLEXSPI\_A\_SCLK | 1 | NVCC\_NAND, 1V8, Input with PD | N25 | NAND\_ALE |
| J6 | Pin44 | QSPIA\_nSS0 | FLEXSPI\_A\_SS0\_B | 1 | NVCC\_NAND, 1V8, Input with PD | L26 | NAND\_CE0\_B |

**4.12 PWM**

DEBIX SOM A exports up to 4 General Purpose Pulse Width Modulators(PWM)

The following features characterize the PWM:

* 16-bit up-counter with clock source selection
* 4 x 16 FIFO to minimize interrupt overhead
* 12-bit prescaler for division of clock
* Sound and melody generation
* Active high or active low configured output
* Can be programmed to be active in low-power mode
* Can be programmed to be active in debug mode
* Interrupts at compare and rollover

**4.12.1 PWM signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin7 | GPIO1\_IO01 | PWM1\_OUT | 1 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset | E8 | GPIO1\_IO01 |
| J5 | Pin70 | SPDIF\_EXT\_CLK | PWM1\_OUT | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC18 | SPDIF\_EXT\_CLK |
| J5 | Pin13 | I2C4\_SDA | PWM1\_OUT | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AD8 | I2C4\_SDA |
| J3 | Pin18 | GPIO1\_IO08 | PWM1\_OUT | 2 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J5 | Pin50 | SAI5\_MCLK | PWM1\_OUT | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin68 | SPDIF\_RX | PWM2\_OUT | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J5 | Pin11 | I2C4\_SCL | PWM2\_OUT | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AF8 | I2C4\_SCL |
| J3 | Pin16 | GPIO1\_IO09 | PWM2\_OUT | 2 | NVCC\_GPIO, 1V8, Input with PD | B8 | GPIO1\_IO09 |
| J3 | Pin12 | GPIO1\_IO11 | PWM2\_OUT | 2 | NVCC\_GPIO, 1V8, Input with PD | D8 | GPIO1\_IO11 |
| J5 | Pin39 | SAI5\_RXD0 | PWM2\_OUT | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J3 | Pin8 | GPIO1\_IO13 | PWM2\_OUT | 5 | NVCC\_GPIO, 1V8, Input with PD | A6 | GPIO1\_IO13 |
| J5 | Pin66 | SPDIF\_TX | PWM3\_OUT | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J5 | Pin9 | I2C3\_SDA | PWM3\_OUT | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ6 | I2C3\_SDA |
| J3 | Pin14 | GPIO1\_IO10 | PWM3\_OUT | 2 | NVCC\_GPIO, 1V8, Input with PD | B7 | GPIO1\_IO10 |
| J5 | Pin48 | SAI5\_RXC | PWM3\_OUT | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J3 | Pin6 | GPIO1\_IO14 | PWM3\_OUT | 5 | NVCC\_GPIO, 1V8, Input with PD | A4 | GPIO1\_IO14 |
| J5 | Pin58 | SAI3\_MCLK | PWM4\_OUT | 1 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |
| J5 | Pin7 | I2C3\_SCL | PWM4\_OUT | 1 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ7 | I2C3\_SCL |
| J5 | Pin46 | SAI5\_RXFS | PWM4\_OUT | 2 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC14 | SAI5\_RXFS |
| J3 | Pin4 | GPIO1\_IO15 | PWM4\_OUT | 5 | NVCC\_GPIO, 1V8, Input with PD | B5 | GPIO1\_IO15 |

**4.13 I2C**

DEBIX SOM A exposes 6 I2C interfaces, I2C1 is used for PMU, it’s not allowed to be configured.

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

* Compatibility with I2C bus standard
* Multimaster operation
* Software programmability for one of 64 different serial clock frequencies
* Software-selectable acknowledge bit
* Interrupt-driven, byte-by-byte data transfer
* Arbitration-lost interrupt with automatic mode switching from master to slave
* Calling address identification interrupt
* Start and stop signal generation/detection
* Repeated Start signal generation
* Acknowledge bit generation/detection
* Bus-busy detection

**4.13.1 I2C1 Signals**

I2C1 is used to communicate with the PMIC on the SOM, it’s NOT allowed to be configured.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin78 | UART3\_RXD | I2C1\_SCL | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF20 | ECSPI1\_SCLK |
| J4 | Pin72 | SD1\_DATA4 | I2C1\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | U26 | SD1\_DATA4 |
| J5 | Pin76 | UART3\_TXD | I2C1\_SDA | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC20 | ECSPI1\_MOSI |
| J4 | Pin74 | SD1\_DATA5 | I2C1\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | AA29 | SD1\_DATA5 |

**4.13.2 I2C2 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin3 | I2C2\_SCL | I2C2\_SCL | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AH6 | I2C2\_SCL |
| J5 | Pin72 | UART3\_CTS | I2C2\_SCL | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD20 | ECSPI1\_MISO |
| J4 | Pin76 | SD1\_DATA6 | I2C2\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | AA28 | SD1\_DATA6 |
| J5 | Pin5 | I2C2\_SDA | I2C2\_SDA | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AE8 | I2C2\_SDA |
| J5 | Pin74 | UART3\_RTS | I2C2\_SDA | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE20 | ECSPI1\_SS0 |
| J4 | Pin78 | SD1\_DATA7 | I2C2\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | U25 | SD1\_DATA7 |

**4.13.3 I2C3 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin7 | I2C3\_SCL | I2C3\_SCL | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AJ7 | I2C3\_SCL |
| J5 | Pin63 | ECSPI2\_SCLK | I2C3\_SCL | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH21 | ECSPI2\_SCLK |
| J4 | Pin65 | SD1\_RESET\_B | I2C3\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | W25 | SD1\_RESET\_B |
| J4 | Pin34 | NAND\_DQS | I2C3\_SCL | 4 | NVCC\_NAND, 1V8, Input with PD | R26 | NAND\_DQS |
| J5 | Pin9 | I2C3\_SDA | I2C3\_SDA | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AJ6 | I2C3\_SDA |
| J5 | Pin67 | ECSPI2\_MOSI | I2C3\_SDA | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ21 | ECSPI2\_MOSI |
| J4 | Pin63 | SD1\_STROBE | I2C3\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | W26 | SD1\_STROBE |

**4.13.4 I2C4 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin11 | I2C4\_SCL | I2C4\_SCL | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AF8 | I2C4\_SCL |
| J6 | Pin35 | SD2\_DATA1 | I2C4\_SCL | 2 | NVCC\_SD2, 1V8, Input with PD | AC29 | SD2\_DATA1 |
| J5 | Pin69 | ECSPI2\_MISO | I2C4\_SCL | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J4 | Pin75 | SD1\_DATA2 | I2C4\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | V29 | SD1\_DATA2 |
| J5 | Pin13 | I2C4\_SDA | I2C4\_SDA | 0 | NVCC\_I2C\_UART, 1V8, Input with PD，already connected to VDD\_1V8 through PU resistor 4.7K | AD8 | I2C4\_SDA |
| J6 | Pin33 | SD2\_DATA0 | I2C4\_SDA | 2 | NVCC\_SD2, 1V8, Input with PD | AC28 | SD2\_DATA0 |
| J5 | Pin65 | ECSPI2\_SS0 | I2C4\_SDA | 2 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ22 | ECSPI2\_SS0 |
| J4 | Pin77 | SD1\_DATA3 | I2C4\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | V28 | SD1\_DATA3 |
| J6 | Pin50 | QSPIA\_DATA2 | I2C4\_SDA | 4 | NVCC\_NAND, 1V8, Input with PD | L24 | NAND\_DATA02 |

**4.13.5 I2C5 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin66 | SPDIF\_TX | I2C5\_SCL | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J4 | Pin67 | SD1\_CLK | I2C5\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | W28 | SD1\_CLK |
| J5 | Pin39 | SAI5\_RXD0 | I2C5\_SCL | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J5 | Pin71 | HDMI\_DDC\_SCL | I2C5\_SCL | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC22 | HDMI\_DDC\_SCL |
| J5 | Pin68 | SPDIF\_RX | I2C5\_SDA | 2 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J4 | Pin69 | SD1\_CMD | I2C5\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | W29 | SD1\_CMD |
| J5 | Pin50 | SAI5\_MCLK | I2C5\_SDA | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin73 | HDMI\_DDC\_SDA | I2C5\_SDA | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF22 | HDMI\_DDC\_SDA |

**4.13.6 I2C6 signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J4 | Pin71 | SD1\_DATA0 | I2C6\_SCL | 3 | NVCC\_SD1, 1V8, Input with PD | Y29 | SD1\_DATA0 |
| J5 | Pin46 | SAI5\_RXFS | I2C6\_SCL | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC14 | SAI5\_RXFS |
| J5 | Pin77 | HDMI\_CEC | I2C6\_SCL | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD22 | HDMI\_CEC |
| J5 | Pin18 | UART4\_RXD | I2C6\_SCL | 4 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |
| J4 | Pin73 | SD1\_DATA1 | I2C6\_SDA | 3 | NVCC\_SD1, 1V8, Input with PD | Y28 | SD1\_DATA1 |
| J5 | Pin48 | SAI5\_RXC | I2C6\_SDA | 3 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J5 | Pin75 | HDMI\_HPD | I2C6\_SDA | 3 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE22 | HDMI\_HPD |
| J5 | Pin16 | UART4\_TXD | I2C6\_SDA | 4 | NVCC\_I2C\_UART, 1V8, Input with PD | AH5 | UART4\_TXD |

**4.14 General Purpose Timer**

DEBIX SOM A exposes GPT interface to its connectors

GPT features are as below:

* One 32-bit up-counter with clock source selection, including external clock.
* Two input capture channels with a programmable trigger edge.
* Three output compare channels with a programmable output mode. A "forced compare" feature is also available.
* Can be programmed to be active in low power and debug modes.
* Interrupt generation at capture, compare, and rollover events.
* Restart or free-run modes for counter operations.

**4.14.1 GPT signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin55 | SAI3\_TXC | GPT1\_CAPTURE1 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J5 | Pin16 | UART4\_TXD | GPT1\_CAPTURE1 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AH5 | UART4\_TXD |
| J5 | Pin59 | SAI3\_TXD | GPT1\_CAPTURE2 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J5 | Pin8 | UART1\_CTS | GPT1\_CAPTURE2 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AE6 | UART3\_RXD |
| J5 | Pin60 | SAI3\_RXC | GPT1\_CLK | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin10 | UART1\_RTS | GPT1\_CLK | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ4 | UART3\_TXD |
| J5 | Pin66 | SPDIF\_TX | GPT1\_COMPARE1 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J5 | Pin18 | UART4\_RXD | GPT1\_COMPARE1 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |
| J5 | Pin68 | SPDIF\_RX | GPT1\_COMPARE2 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J5 | Pin12 | UART2\_TXD | GPT1\_COMPARE2 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AH4 | UART2\_TXD |
| J5 | Pin70 | SPDIF\_EXT\_CLK | GPT1\_COMPARE3 | 3 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC18 | SPDIF\_EXT\_CLK |
| J5 | Pin14 | UART2\_RXD | GPT1\_COMPARE3 | 3 | NVCC\_I2C\_UART, 1V8, Input with PD | AF6 | UART2\_RXD |
| J5 | Pin7 | I2C3\_SCL | GPT2\_CLK | 2 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ7 | I2C3\_SCL |
| J5 | Pin9 | I2C3\_SDA | GPT3\_CLK | 2 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ6 | I2C3\_SDA |

**4.15 Reference Clocks**

DEBIX SOM A exposes several clock outputs from its CCM module, these signals can be used to clock external devices

**4.15.1 Clock signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J5 | Pin69 | ECSPI2\_MISO | CCM\_CLKO1 | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J3 | Pin6 | GPIO1\_IO14 | CCM\_CLKO1 | 6 | NVCC\_GPIO, 1V8, Input with PD | A4 | GPIO1\_IO14 |
| J5 | Pin65 | ECSPI2\_SS0 | CCM\_CLKO2 | 4 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ22 | ECSPI2\_SS0 |
| J3 | Pin4 | GPIO1\_IO15 | CCM\_CLKO2 | 6 | NVCC\_GPIO, 1V8, Input with PD | B5 | GPIO1\_IO15 |
| J3 | Pin9 | GPIO1\_IO00 | CCM\_ENET\_PHY\_REF\_CLK\_ROOT | 1 | NVCC\_GPIO, 1V8, Input with PD | A7 | GPIO1\_IO00 |
| J6 | Pin16 | ENET\_TD2 | CCM\_ENET\_QOS\_CLOCK\_GENERATE\_REF\_CLK | 1 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J5 | Pin42 | SAI1\_MCLK | ENET1\_TX\_CLK | 4 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE12 | SAI1\_MCLK |
| J3 | Pin9 | GPIO1\_IO00 | CCM\_EXT\_CLK1 | 6 | NVCC\_GPIO, 1V8, Input with PD | A7 | GPIO1\_IO00 |
| J3 | Pin7 | GPIO1\_IO01 | CCM\_EXT\_CLK2 | 6 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset | E8 | GPIO1\_IO01 |
| J3 | Pin3 | GPIO1\_IO06 | CCM\_EXT\_CLK3 | 6 | NVCC\_GPIO, 1V8, Input with PD | A3 | GPIO1\_IO06 |
| J3 | Pin20 | GPIO1\_IO07 | CCM\_EXT\_CLK4 | 6 | NVCC\_GPIO, 1V8, Input with PD | F6 | GPIO1\_IO07 |
| J3 | Pin9 | GPIO1\_IO00 | CCM\_EXT\_CLK1 | 5 | NVCC\_GPIO, 1V8, Input with PD | A7 | GPIO1\_IO00 |
| J4 | Pin56 | CLKIN1 |  |  | NVCC\_CLK, 1V8, Input with PD | K28 | CLKIN1 |
| J4 | Pin64 | CLKIN2 |  |  | NVCC\_CLK, 1V8, Input with PD | L28 | CLKIN2 |
| J4 | Pin60 | CLKOUT1 |  |  | NVCC\_CLK, 1V8, Output low | K29 | CLKOUT1 |
| J4 | Pin68 | CLKOUT2 |  |  | NVCC\_CLK, 1V8, Output low | L29 | CLKOUT2 |

**4.16 JTAG**

DEBIX SOM A exposes Secure JTAG Controller(SJC), which provides maximum security for debug and test.

JTAG interface(Joint Test Action Group), is an international standard test protocol(be compatible with IEEE 1149.1), mainly used for chip internal test.

JTAG standard defines a serial shift register. Each cell of this register is allocated to the corresponding IC chip pin. Each separate cell is called BSC(Boundary-Scan Cell). The serially-connected BSC constructs JTAG return circuit, all the BSR(Boundary-Scan Register) is activated by JTAG test.

DEBIX SOM A JTAG\_MOD pin is bind to low so that it can be configured as Daisy chain ALL mode for SW debug(high speed and production)

**4.16.1 JTAG signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin46 | JTAG\_MOD | JTAG\_MOD | 0 | NVCC\_JTAG, 1V8, Input with PD | G20 | JTAG\_MOD |
| J3 | Pin48 | JTAG\_TCK | JTAG\_TCK | 0 | NVCC\_JTAG, 1V8, Input with PU | G18 | JTAG\_TCK |
| J3 | Pin44 | JTAG\_TDI | JTAG\_TDI | 0 | NVCC\_JTAG, 1V8, Input with PU | G16 | JTAG\_TDI |
| J3 | Pin42 | JTAG\_TDO | JTAG\_TDO | 0 | NVCC\_JTAG, 1V8, Input with PU | F14 | JTAG\_TDO |
| J3 | Pin40 | JTAG\_TMS | JTAG\_TMS | 0 | NVCC\_JTAG, 1V8, Input with PU | G14 | JTAG\_TMS |
| J4 | Pin52 | WDOG\_B | SJC\_DE\_B | 7 | NVCC\_GPIO, 1V8, Input with PU | B6 | GPIO1\_IO02 |

**4.17 General Purpose IO**

DEBIX SOM A provides pins that can be configured as GPIOs

**4.17.1 GPIO signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin9 | GPIO1\_IO00 | GPIO1\_IO00 | 0 | NVCC\_GPIO, 1V8, Input with PD | A7 | GPIO1\_IO00 |
| J3 | Pin7 | GPIO1\_IO01 | GPIO1\_IO01 | 0 | NVCC\_GPIO, 1V8, Output low during reset, input with PD after reset | E8 | GPIO1\_IO01 |
| J4 | Pin52 | WDOG\_B | GPIO1\_IO02 | 0 | NVCC\_GPIO, 1V8, Input with PU | B6 | GPIO1\_IO02 |
| J3 | Pin5 | GPIO1\_IO05 | GPIO1\_IO05 | 0 | NVCC\_GPIO, 1V8, Output high during reset, input with PU after reset | B4 | GPIO1\_IO05 |
| J3 | Pin3 | GPIO1\_IO06 | GPIO1\_IO06 | 0 | NVCC\_GPIO, 1V8, Input with PD | A3 | GPIO1\_IO06 |
| J3 | Pin20 | GPIO1\_IO07 | GPIO1\_IO07 | 0 | NVCC\_GPIO, 1V8, Input with PD | F6 | GPIO1\_IO07 |
| J3 | Pin18 | GPIO1\_IO08 | GPIO1\_IO08 | 0 | NVCC\_GPIO, 1V8, Input with PD | A8 | GPIO1\_IO08 |
| J3 | Pin16 | GPIO1\_IO09 | GPIO1\_IO09 | 0 | NVCC\_GPIO, 1V8, Input with PD | B8 | GPIO1\_IO09 |
| J3 | Pin14 | GPIO1\_IO10 | GPIO1\_IO10 | 0 | NVCC\_GPIO, 1V8, Input with PD | B7 | GPIO1\_IO10 |
| J3 | Pin12 | GPIO1\_IO11 | GPIO1\_IO11 | 0 | NVCC\_GPIO, 1V8, Input with PD | D8 | GPIO1\_IO11 |
| J3 | Pin10 | GPIO1\_IO12 | GPIO1\_IO12 | 0 | NVCC\_GPIO, 1V8, Input with PD | A5 | GPIO1\_IO12 |
| J3 | Pin8 | GPIO1\_IO13 | GPIO1\_IO13 | 0 | NVCC\_GPIO, 1V8, Input with PD | A6 | GPIO1\_IO13 |
| J3 | Pin6 | GPIO1\_IO14 | GPIO1\_IO14 | 0 | NVCC\_GPIO, 1V8, Input with PD | A4 | GPIO1\_IO14 |
| J3 | Pin4 | GPIO1\_IO15 | GPIO1\_IO15 | 0 | NVCC\_GPIO, 1V8, Input with PD | B5 | GPIO1\_IO15 |
| J6 | Pin4 | ENET\_MDC | GPIO1\_IO16 | 5 | NVCC\_ENET, 1V8, Input with PD | AH28 | ENET\_MDC |
| J6 | Pin6 | ENET\_MDIO | GPIO1\_IO17 | 5 | NVCC\_ENET, 1V8, Input with PD | AH29 | ENET\_MDIO |
| J6 | Pin18 | ENET\_TD3 | GPIO1\_IO18 | 5 | NVCC\_ENET, 1V8, Input with PD | AD24 | ENET\_TD3 |
| J6 | Pin16 | ENET\_TD2 | GPIO1\_IO19 | 5 | NVCC\_ENET, 1V8, Input with PD | AF26 | ENET\_TD2 |
| J6 | Pin14 | ENET\_TD1 | GPIO1\_IO20 | 5 | NVCC\_ENET, 1V8, Input with PD | AE26 | ENET\_TD1 |
| J6 | Pin12 | ENET\_TD0 | GPIO1\_IO21 | 5 | NVCC\_ENET, 1V8, Input with PD | AC25 | ENET\_TD0 |
| J6 | Pin8 | ENET\_TX\_CTL | GPIO1\_IO22 | 5 | NVCC\_ENET, 1V8, Input with PD | AF24 | ENET\_TX\_CTL |
| J6 | Pin10 | ENET\_TXC | GPIO1\_IO23 | 5 | NVCC\_ENET, 1V8, Input with PD | AE24 | ENET\_TXC |
| J6 | Pin20 | ENET\_RX\_CTL | GPIO1\_IO24 | 5 | NVCC\_ENET, 1V8, Input with PD | AE28 | ENET\_RX\_CTL |
| J6 | Pin22 | ENET\_RXC | GPIO1\_IO25 | 5 | NVCC\_ENET, 1V8, Input with PD | AE29 | ENET\_RXC |
| J6 | Pin24 | ENET\_RD0 | GPIO1\_IO26 | 5 | NVCC\_ENET, 1V8, Input with PD | AG29 | ENET\_RD0 |
| J6 | Pin26 | ENET\_RD1 | GPIO1\_IO27 | 5 | NVCC\_ENET, 1V8, Input with PD | AG28 | ENET\_RD1 |
| J6 | Pin28 | ENET\_RD2 | GPIO1\_IO28 | 5 | NVCC\_ENET, 1V8, Input with PD | AF29 | ENET\_RD2 |
| J6 | Pin30 | ENET\_RD3 | GPIO1\_IO29 | 5 | NVCC\_ENET, 1V8, Input with PD | AF28 | ENET\_RD3 |
| J4 | Pin67 | SD1\_CLK | GPIO2\_IO00 | 5 | NVCC\_SD1, 1V8, Input with PD | W28 | SD1\_CLK |
| J4 | Pin69 | SD1\_CMD | GPIO2\_IO01 | 5 | NVCC\_SD1, 1V8, Input with PD | W29 | SD1\_CMD |
| J4 | Pin71 | SD1\_DATA0 | GPIO2\_IO02 | 5 | NVCC\_SD1, 1V8, Input with PD | Y29 | SD1\_DATA0 |
| J4 | Pin73 | SD1\_DATA1 | GPIO2\_IO03 | 5 | NVCC\_SD1, 1V8, Input with PD | Y28 | SD1\_DATA1 |
| J4 | Pin75 | SD1\_DATA2 | GPIO2\_IO04 | 5 | NVCC\_SD1, 1V8, Input with PD | V29 | SD1\_DATA2 |
| J4 | Pin77 | SD1\_DATA3 | GPIO2\_IO05 | 5 | NVCC\_SD1, 1V8, Input with PD | V28 | SD1\_DATA3 |
| J4 | Pin72 | SD1\_DATA4 | GPIO2\_IO06 | 5 | NVCC\_SD1, 1V8, Input with PD | U26 | SD1\_DATA4 |
| J4 | Pin74 | SD1\_DATA5 | GPIO2\_IO07 | 5 | NVCC\_SD1, 1V8, Input with PD | AA29 | SD1\_DATA5 |
| J4 | Pin76 | SD1\_DATA6 | GPIO2\_IO08 | 5 | NVCC\_SD1, 1V8, Input with PD | AA28 | SD1\_DATA6 |
| J4 | Pin78 | SD1\_DATA7 | GPIO2\_IO09 | 5 | NVCC\_SD1, 1V8, Input with PD | U25 | SD1\_DATA7 |
| J4 | Pin65 | SD1\_RESET\_B | GPIO2\_IO10 | 5 | NVCC\_SD1, 1V8, Input with PD | W25 | SD1\_RESET\_B |
| J4 | Pin63 | SD1\_STROBE | GPIO2\_IO11 | 5 | NVCC\_SD1, 1V8, Input with PD | W26 | SD1\_STROBE |
| J6 | Pin36 | SD2\_nCD | GPIO2\_IO12 | 5 | NVCC\_SD2, 1V8, Input with PD | AD29 | SD2\_CD\_B |
| J6 | Pin38 | SD2\_CLK | GPIO2\_IO13 | 5 | NVCC\_SD2, 1V8, Input with PD | AB29 | SD2\_CLK |
| J6 | Pin40 | SD2\_CMD | GPIO2\_IO14 | 5 | NVCC\_SD2, 1V8, Input with PD | AB28 | SD2\_CMD |
| J6 | Pin33 | SD2\_DATA0 | GPIO2\_IO15 | 5 | NVCC\_SD2, 1V8, Input with PD | AC28 | SD2\_DATA0 |
| J6 | Pin35 | SD2\_DATA1 | GPIO2\_IO16 | 5 | NVCC\_SD2, 1V8, Input with PD | AC29 | SD2\_DATA1 |
| J6 | Pin37 | SD2\_DATA2 | GPIO2\_IO17 | 5 | NVCC\_SD2, 1V8, Input with PD | AA26 | SD2\_DATA2 |
| J6 | Pin42 | SD2\_DATA3 | GPIO2\_IO18 | 5 | NVCC\_SD2, 1V8, Input with PD | AA25 | SD2\_DATA3 |
| J6 | Pin34 | SD2\_WP | GPIO2\_IO20 | 5 | NVCC\_SD2, 1V8, Input with PD | AC26 | SD2\_WP |
| J6 | Pin41 | QSPIA\_SCLK | GPIO3\_IO00 | 5 | NVCC\_NAND, 1V8, Input with PD | N25 | NAND\_ALE |
| J6 | Pin44 | QSPIA\_nSS0 | GPIO3\_IO01 | 5 | NVCC\_NAND, 1V8, Input with PD | L26 | NAND\_CE0\_B |
| J6 | Pin46 | QSPIA\_DATA0 | GPIO3\_IO06 | 5 | NVCC\_NAND, 1V8, Input with PD | R25 | NAND\_DATA00 |
| J6 | Pin48 | QSPIA\_DATA1 | GPIO3\_IO07 | 5 | NVCC\_NAND, 1V8, Input with PD | L25 | NAND\_DATA01 |
| J6 | Pin50 | QSPIA\_DATA2 | GPIO3\_IO08 | 5 | NVCC\_NAND, 1V8, Input with PD | L24 | NAND\_DATA02 |
| J6 | Pin52 | QSPIA\_DATA3 | GPIO3\_IO09 | 5 | NVCC\_NAND, 1V8, Input with PD | N24 | NAND\_DATA03 |
| J4 | Pin34 | NAND\_DQS | GPIO3\_IO14 | 5 | NVCC\_NAND, 1V8, Input with PD | R26 | NAND\_DQS |
| J5 | Pin46 | SAI5\_RXFS | GPIO3\_IO19 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC14 | SAI5\_RXFS |
| J5 | Pin48 | SAI5\_RXC | GPIO3\_IO20 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD14 | SAI5\_RXC |
| J5 | Pin39 | SAI5\_RXD0 | GPIO3\_IO21 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE16 | SAI5\_RXD0 |
| J5 | Pin41 | SAI5\_RXD1 | GPIO3\_IO22 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD16 | SAI5\_RXD1 |
| J5 | Pin43 | SAI5\_RXD2 | GPIO3\_IO23 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF16 | SAI5\_RXD2 |
| J5 | Pin45 | SAI5\_RXD3 | GPIO3\_IO24 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE14 | SAI5\_RXD3 |
| J5 | Pin50 | SAI5\_MCLK | GPIO3\_IO25 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF14 | SAI5\_MCLK |
| J5 | Pin71 | HDMI\_DDC\_SCL | GPIO3\_IO26 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC22 | HDMI\_DDC\_SCL |
| J5 | Pin73 | HDMI\_DDC\_SDA | GPIO3\_IO27 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF22 | HDMI\_DDC\_SDA |
| J5 | Pin77 | HDMI\_CEC | GPIO3\_IO28 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD22 | HDMI\_CEC |
| J5 | Pin75 | HDMI\_HPD | GPIO3\_IO29 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE22 | HDMI\_HPD |
| J5 | Pin22 | SAI1\_RXFS | GPIO4\_IO00 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ9 | SAI1\_RXFS |
| J5 | Pin24 | SAI1\_RXC | GPIO4\_IO01 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH8 | SAI1\_RXC |
| J5 | Pin26 | SAI1\_RXD0 | GPIO4\_IO02 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC10 | SAI1\_RXD0 |
| J5 | Pin28 | SAI1\_RXD1 | GPIO4\_IO03 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF10 | SAI1\_RXD1 |
| J5 | Pin30 | SAI1\_RXD2 | GPIO4\_IO04 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH9 | SAI1\_RXD2 |
| J5 | Pin32 | SAI1\_RXD3 | GPIO4\_IO05 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ8 | SAI1\_RXD3 |
| J5 | Pin34 | SAI1\_RXD4 | GPIO4\_IO06 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD10 | SAI1\_RXD4 |
| J5 | Pin36 | SAI1\_RXD5 | GPIO4\_IO07 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE10 | SAI1\_RXD5 |
| J5 | Pin38 | SAI1\_RXD6 | GPIO4\_IO08 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH10 | SAI1\_RXD6 |
| J5 | Pin40 | SAI1\_RXD7 | GPIO4\_IO09 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH12 | SAI1\_RXD7 |
| J5 | Pin35 | SAI1\_TXFS | GPIO4\_IO10 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AF12 | SAI1\_TXFS |
| J5 | Pin17 | SAI1\_TXC | GPIO4\_IO11 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ12 | SAI1\_TXC |
| J5 | Pin19 | SAI1\_TXD0 | GPIO4\_IO12 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ11 | SAI1\_TXD0 |
| J5 | Pin21 | SAI1\_TXD1 | GPIO4\_IO13 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ10 | SAI1\_TXD1 |
| J5 | Pin23 | SAI1\_TXD2 | GPIO4\_IO14 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH11 | SAI1\_TXD2 |
| J5 | Pin25 | SAI1\_TXD3 | GPIO4\_IO15 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AD12 | SAI1\_TXD3 |
| J5 | Pin27 | SAI1\_TXD4 | GPIO4\_IO16 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH13 | SAI1\_TXD4 |
| J5 | Pin29 | SAI1\_TXD5 | GPIO4\_IO17 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH14 | SAI1\_TXD5 |
| J5 | Pin31 | SAI1\_TXD6 | GPIO4\_IO18 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AC12 | SAI1\_TXD6 |
| J5 | Pin33 | SAI1\_TXD7 | GPIO4\_IO19 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ13 | SAI1\_TXD7 |
| J5 | Pin42 | SAI1\_MCLK | GPIO4\_IO20 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AE12 | SAI1\_MCLK |
| J5 | Pin52 | SAI2\_RXFS | GPIO4\_IO21 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AH17 | SAI2\_RXFS |
| J5 | Pin54 | SAI2\_RXC | GPIO4\_IO22 | 5 | NVCC\_SAI1\_SAI5, 1V8, Input with PD | AJ16 | SAI2\_RXC |
| J5 | Pin53 | SAI2\_RXD | GPIO4\_IO23 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ14 | SAI2\_RXD0 |
| J5 | Pin49 | SAI2\_TXFS | GPIO4\_IO24 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ17 | SAI2\_TXFS |
| J5 | Pin47 | SAI2\_TXC | GPIO4\_IO25 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH15 | SAI2\_TXC |
| J5 | Pin51 | SAI2\_TXD | GPIO4\_IO26 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH16 | SAI2\_TXD0 |
| J5 | Pin56 | SAI2\_MCLK | GPIO4\_IO27 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ15 | SAI2\_MCLK |
| J5 | Pin62 | SAI3\_RXFS | GPIO4\_IO28 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ19 | SAI3\_RXFS |
| J5 | Pin60 | SAI3\_RXC | GPIO4\_IO29 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ18 | SAI3\_RXC |
| J5 | Pin64 | SAI3\_RXD | GPIO4\_IO30 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AF18 | SAI3\_RXD |
| J5 | Pin57 | SAI3\_TXFS | GPIO4\_IO31 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC16 | SAI3\_TXFS |
| J5 | Pin55 | SAI3\_TXC | GPIO5\_IO00 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH19 | SAI3\_TXC |
| J5 | Pin59 | SAI3\_TXD | GPIO5\_IO01 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AH18 | SAI3\_TXD |
| J5 | Pin58 | SAI3\_MCLK | GPIO5\_IO02 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AJ20 | SAI3\_MCLK |
| J5 | Pin66 | SPDIF\_TX | GPIO5\_IO03 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AE18 | SPDIF\_TX |
| J5 | Pin68 | SPDIF\_RX | GPIO5\_IO04 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AD18 | SPDIF\_RX |
| J5 | Pin70 | SPDIF\_EXT\_CLK | GPIO5\_IO05 | 5 | NVCC\_SAI2\_SAI3\_SPDIF, 1V8, Input with PD | AC18 | SPDIF\_EXT\_CLK |
| J5 | Pin78 | UART3\_RXD | GPIO5\_IO06 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AF20 | ECSPI1\_SCLK |
| J5 | Pin76 | UART3\_TXD | GPIO5\_IO07 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AC20 | ECSPI1\_MOSI |
| J5 | Pin72 | UART3\_CTS | GPIO5\_IO08 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AD20 | ECSPI1\_MISO |
| J5 | Pin74 | UART3\_RTS | GPIO5\_IO09 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AE20 | ECSPI1\_SS0 |
| J5 | Pin63 | ECSPI2\_SCLK | GPIO5\_IO10 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH21 | ECSPI2\_SCLK |
| J5 | Pin67 | ECSPI2\_MOSI | GPIO5\_IO11 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ21 | ECSPI2\_MOSI |
| J5 | Pin69 | ECSPI2\_MISO | GPIO5\_IO12 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AH20 | ECSPI2\_MISO |
| J5 | Pin65 | ECSPI2\_SS0 | GPIO5\_IO13 | 5 | NVCC\_ECSPI\_HDMI, 1V8, Input with PD | AJ22 | ECSPI2\_SS0 |
| J5 | Pin3 | I2C2\_SCL | GPIO5\_IO16 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AH6 | I2C2\_SCL |
| J5 | Pin5 | I2C2\_SDA | GPIO5\_IO17 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AE8 | I2C2\_SDA |
| J5 | Pin7 | I2C3\_SCL | GPIO5\_IO18 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ7 | I2C3\_SCL |
| J5 | Pin9 | I2C3\_SDA | GPIO5\_IO19 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ6 | I2C3\_SDA |
| J5 | Pin11 | I2C4\_SCL | GPIO5\_IO20 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AF8 | I2C4\_SCL |
| J5 | Pin13 | I2C4\_SDA | GPIO5\_IO21 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AD8 | I2C4\_SDA |
| J5 | Pin6 | UART1\_RXD | GPIO5\_IO22 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AD6 | UART1\_RXD |
| J5 | Pin4 | UART1\_TXD | GPIO5\_IO23 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ3 | UART1\_TXD |
| J5 | Pin14 | UART2\_RXD | GPIO5\_IO24 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AF6 | UART2\_RXD |
| J5 | Pin12 | UART2\_TXD | GPIO5\_IO25 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AH4 | UART2\_TXD |
| J5 | Pin8 | UART1\_CTS | GPIO5\_IO26 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AE6 | UART3\_RXD |
| J5 | Pin10 | UART1\_RTS | GPIO5\_IO27 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ4 | UART3\_TXD |
| J5 | Pin18 | UART4\_RXD | GPIO5\_IO28 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AJ5 | UART4\_RXD |
| J5 | Pin16 | UART4\_TXD | GPIO5\_IO29 | 5 | NVCC\_I2C\_UART, 1V8, Input with PD | AH5 | UART4\_TXD |

**4.18 Power**

**4.18.1 Power signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J3 | Pin36 | USB1\_VBUS\_3V3 | USB1\_VBUS | 0 | VDD\_USB\_3P3, 3.3V, Input | A11 | USB1\_VBUS |
| J3 | Pin38 | USB2\_VBUS\_3V3 | USB2\_VBUS | 0 | VDD\_USB\_3P3, 3.3V, Input | D12 | USB2\_VBUS |
| J6 | Pin47 | VSD\_3V3 |  |  |  |  |  |
| J6 | Pin49 | VSD\_3V3 |  |  |  |  |  |
| J6 | Pin51 | VSD\_3V3 |  |  |  |  |  |
| J6 | Pin53 | VDD\_3V3 |  |  |  |  |  |
| J6 | Pin54 | VDD\_1V8 |  |  |  |  |  |
| J6 | Pin55 | VDD\_3V3 |  |  |  |  |  |
| J6 | Pin56 | VDD\_1V8 |  |  |  |  |  |
| J6 | Pin57 | VDD\_3V3 |  |  |  |  |  |
| J6 | Pin58 | VDD\_1V8 |  |  |  |  |  |
| J6 | Pin59 | VDD\_3V3 |  |  |  |  |  |
| J6 | Pin60 | VDD\_1V8 |  |  |  |  |  |
| J6 | Pin71 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin72 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin73 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin74 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin75 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin76 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin77 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin78 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin79 | VSYS\_5V |  |  |  |  |  |
| J6 | Pin80 | VSYS\_5V |  |  |  |  |  |

**4.18.2 Ground**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** |
| J3 | Pin1 | GND |  |  |  |  |
| J3 | Pin2 | GND |  |  |  |  |
| J3 | Pin11 | GND |  |  |  |  |
| J3 | Pin17 | GND |  |  |  |  |
| J3 | Pin22 | GND |  |  |  |  |
| J3 | Pin23 | GND |  |  |  |  |
| J3 | Pin28 | GND |  |  |  |  |
| J3 | Pin29 | GND |  |  |  |  |
| J3 | Pin34 | GND |  |  |  |  |
| J3 | Pin35 | GND |  |  |  |  |
| J3 | Pin41 | GND |  |  |  |  |
| J3 | Pin47 | GND |  |  |  |  |
| J3 | Pin50 | GND |  |  |  |  |
| J3 | Pin53 | GND |  |  |  |  |
| J3 | Pin56 | GND |  |  |  |  |
| J3 | Pin62 | GND |  |  |  |  |
| J3 | Pin63 | GND |  |  |  |  |
| J3 | Pin68 | GND |  |  |  |  |
| J3 | Pin69 | GND |  |  |  |  |
| J3 | Pin74 | GND |  |  |  |  |
| J3 | Pin79 | GND |  |  |  |  |
| J3 | Pin80 | GND |  |  |  |  |
| J4 | Pin1 | GND |  |  |  |  |
| J4 | Pin2 | GND |  |  |  |  |
| J4 | Pin7 | GND |  |  |  |  |
| J4 | Pin8 | GND |  |  |  |  |
| J4 | Pin13 | GND |  |  |  |  |
| J4 | Pin14 | GND |  |  |  |  |
| J4 | Pin19 | GND |  |  |  |  |
| J4 | Pin20 | GND |  |  |  |  |
| J4 | Pin25 | GND |  |  |  |  |
| J4 | Pin26 | GND |  |  |  |  |
| J4 | Pin31 | GND |  |  |  |  |
| J4 | Pin32 | GND |  |  |  |  |
| J4 | Pin37 | GND |  |  |  |  |
| J4 | Pin42 | GND |  |  |  |  |
| J4 | Pin43 | GND |  |  |  |  |
| J4 | Pin49 | GND |  |  |  |  |
| J4 | Pin54 | GND |  |  |  |  |
| J4 | Pin55 | GND |  |  |  |  |
| J4 | Pin58 | GND |  |  |  |  |
| J4 | Pin61 | GND |  |  |  |  |
| J4 | Pin62 | GND |  |  |  |  |
| J4 | Pin66 | GND |  |  |  |  |
| J4 | Pin70 | GND |  |  |  |  |
| J4 | Pin79 | GND |  |  |  |  |
| J4 | Pin80 | GND |  |  |  |  |
| J5 | Pin1 | GND |  |  |  |  |
| J5 | Pin2 | GND |  |  |  |  |
| J5 | Pin15 | GND |  |  |  |  |
| J5 | Pin20 | GND |  |  |  |  |
| J5 | Pin37 | GND |  |  |  |  |
| J5 | Pin44 | GND |  |  |  |  |
| J5 | Pin61 | GND |  |  |  |  |
| J5 | Pin79 | GND |  |  |  |  |
| J5 | Pin80 | GND |  |  |  |  |
| J6 | Pin1 | GND |  |  |  |  |
| J6 | Pin2 | GND |  |  |  |  |
| J6 | Pin7 | GND |  |  |  |  |
| J6 | Pin13 | GND |  |  |  |  |
| J6 | Pin19 | GND |  |  |  |  |
| J6 | Pin25 | GND |  |  |  |  |
| J6 | Pin31 | GND |  |  |  |  |
| J6 | Pin32 | GND |  |  |  |  |
| J6 | Pin39 | GND |  |  |  |  |
| J6 | Pin61 | GND |  |  |  |  |
| J6 | Pin62 | GND |  |  |  |  |
| J6 | Pin63 | GND |  |  |  |  |
| J6 | Pin64 | GND |  |  |  |  |
| J6 | Pin65 | GND |  |  |  |  |
| J6 | Pin66 | GND |  |  |  |  |
| J6 | Pin67 | GND |  |  |  |  |
| J6 | Pin68 | GND |  |  |  |  |
| J6 | Pin69 | GND |  |  |  |  |
| J6 | Pin70 | GND |  |  |  |  |

**4.19 System Control**

**4.19.1 System Control Signals**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J6 | Pin45 | SYS\_nRST |  |  |  |  |  |
| J4 | Pin36 | ONOFF | ONOFF | 0 | NVCC\_SNVS, 1V8, Input with PU | G22 | ONOFF |
| J4 | Pin38 | POR\_B | POR\_B | 0 | NVCC\_SNVS, 1V8, Input with PU | J29 | POR\_B |
| J4 | Pin40 | PMIC\_ON\_REQ | PMIC\_ON\_REQ | 0 | NVCC\_SNVS, 1V8, Output high with PU | F22 | LVDS0\_D1\_P |

**4.19.2 Boot configuration**

DEBIX SOM A can be configured to boot from the following sources:

* Internal source: eMMC Flash memory
* External source: SD card

BOOT\_MODE pins determines the boot source

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Location** | **Pin** | **Default** | **ALT\_NAME** | **ALT#** | **NOTES** | **BALL** | **BALL\_NAME** |
| J4 | Pin44 | BOOT\_MODE0 | BOOT\_MODE0 | 0 | NVCC\_JTAG, 1V8, Input with PD | G10 | BOOT\_MODE0 |
| J4 | Pin46 | BOOT\_MODE1 | BOOT\_MODE1 | 0 | NVCC\_JTAG, 1V8, Input with PD | F8 | BOOT\_MODE1 |
| J4 | Pin48 | BOOT\_MODE2 | BOOT\_MODE2 | 0 | NVCC\_JTAG, 1V8, Input with PD | G8 | BOOT\_MODE2 |
| J4 | Pin50 | BOOT\_MODE3 | BOOT\_MODE3 | 0 | NVCC\_JTAG, 1V8, Input with PD | G12 | BOOT\_MODE3 |

**4.19.3 Boundary Scan**

To enter Boundary Scan BOOT\_MODE0, BOOT\_MODE1, BOOT\_MODE2, BOOT\_MODE3, JTAG\_MOD and PROB\_B need to be pulled to “111111” for i.MX 8M Plus to enter Boundary Scan mode.

**Chapter 5 Electrical specifications**

**5.1 Maximum absolute ratings**

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Min** | **Max** | **Unit** |
| VBAT | -0.3 | 5.5 | V |
| USB\_VBUS | -0.3 | 5.25 | V |

**5.2 operating conditions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Min** | **Typ.** | **Max.** | **Unit** |
| VBAT | 3.5 | 3.8 | 5 | V |

**5.3 Peripheral Voltage levels**

Most peripheral interface lines used as inputs or outputs of DEBIX SOM A use 1.8V LVCMOS levels, please refer to the previous chapters to check the Notes of the specific pins in the instruction tables.

**5.4 Power Consumption**

DEBIX SOM A power consumption

|  |  |  |  |
| --- | --- | --- | --- |
| **Voltage[V]** | **Current[A]** | **Power[W]** | **Conditions** |
| 3.8V | ~0.30A | ~1.14W | Ubuntu suspend |
| 3.8V | ~0.66A | ~2.51W | Ubuntu Stress test, Use the stress tool to test. |

**Note:** Actual power consumption may vary depending on the peripherals DEBIX SOM A is communicating with. Proper thermal solutions should be applied according to the specific use cases.

**Chapter 6 Environmental Specifications**

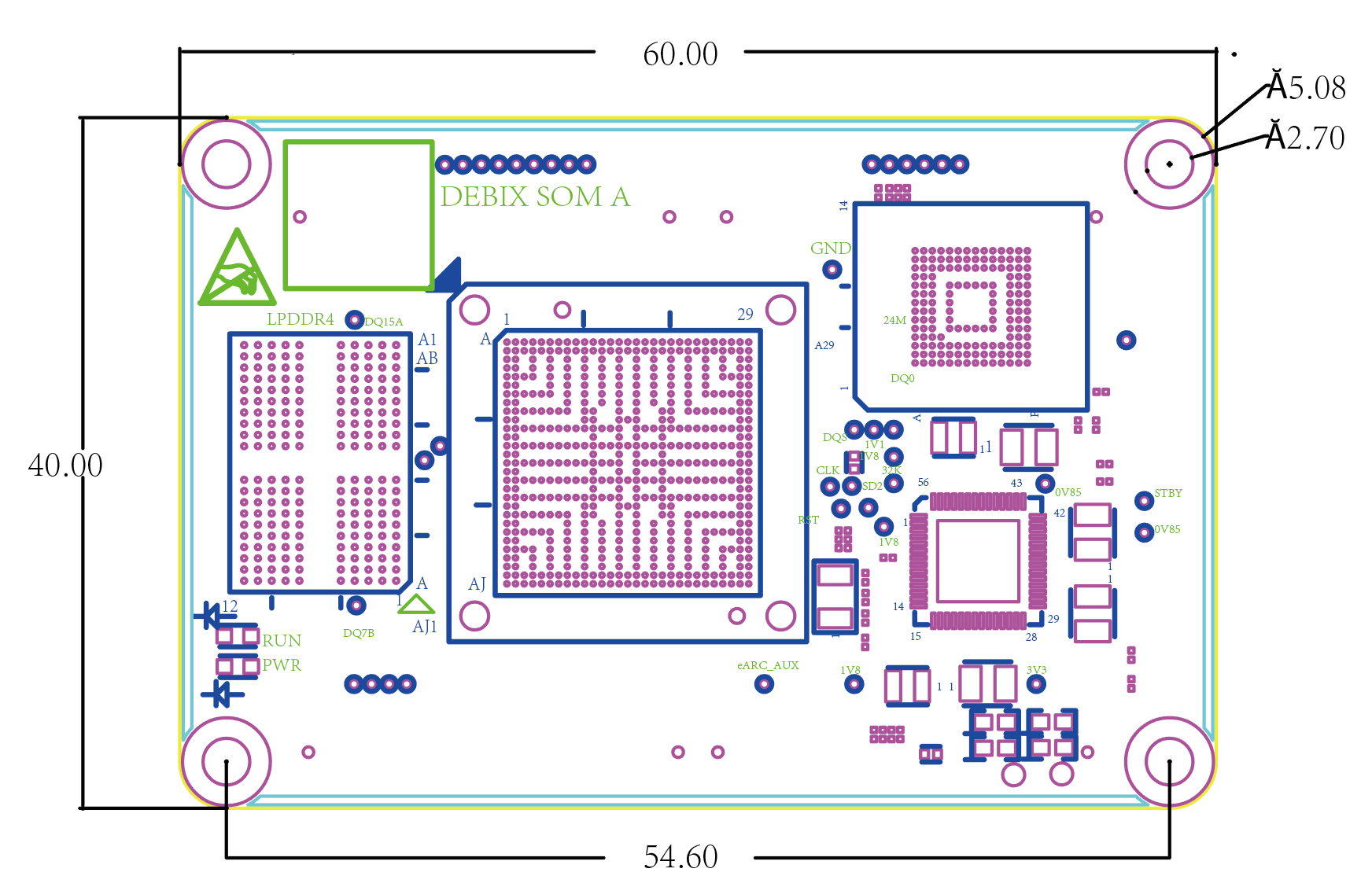
* Commercial Operating Temperature Range: 0℃~70℃
* Extended Operating Temperature Range: -25℃~85℃
* Industrial Operating Temperature Range: -40℃~85℃

**Chapter 7 Mechanical**

**7.1 Carrier board mounting**

DEBIX SOM A has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

**7.2 DEBIX SOM A dimension**



Dimension:

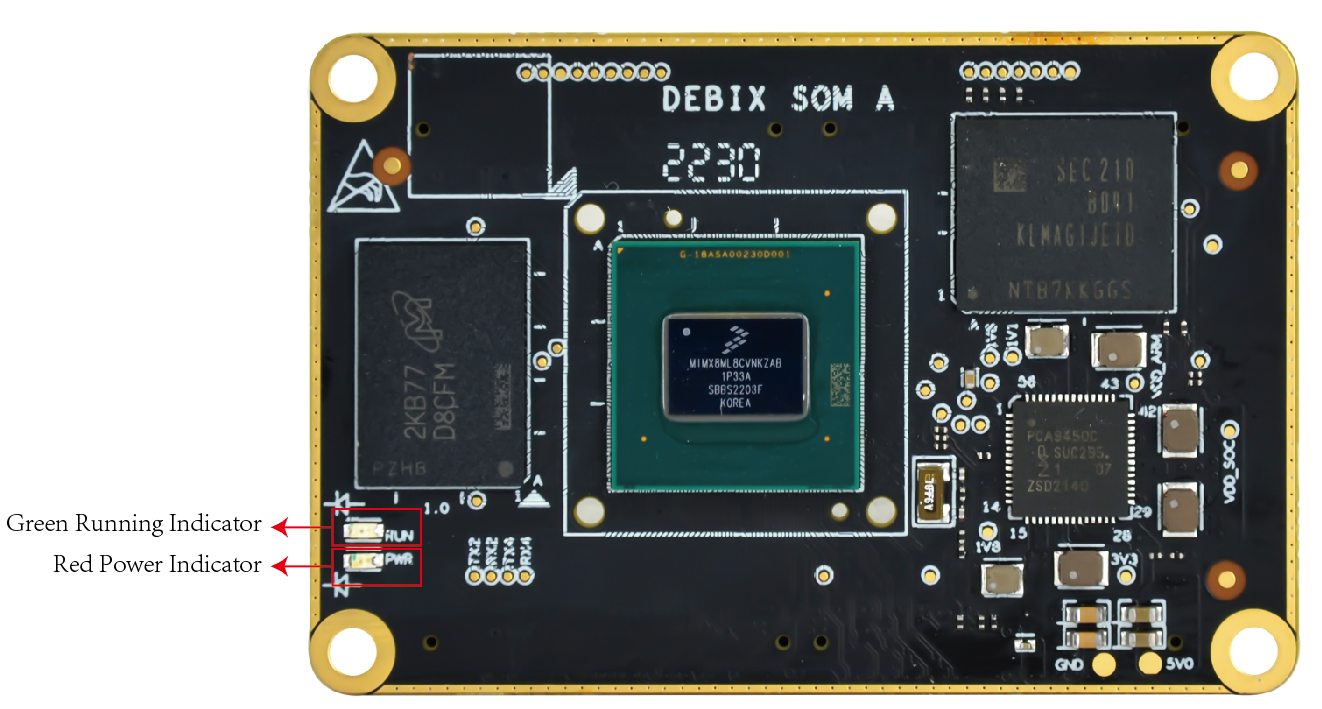
Length: 60mm

Width: 40mm

Height: 5.6mm

CAD files can be accessed from: <https://www.debix.io>

**7.3 Indicators**



* Green indicator: running indicator, can be controlled through software programming, it is blinking by default on DEBIX SOM A
* Red indicator: power indicator, it lights normally if power is normal

**7.4 Thermal Management**

It’s advised using external heat dissipation solutions. The chosen method may vary according to the different mechanical design of the device.